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Thanos et al.

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[54] HIGH PERFORMANCE, HIGH CAPACITY MICRO-WINCHESTER DISK DRIVE

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[73] Assignee: Quantum Corp., Milpitas, Calif.

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[51] Int. Cl.<sup>5</sup> ..... G11B 5/596

[52] U.S. Cl. ..... 360/77.08; 360/77.03; 360/77.04; 360/77.05; 360/78.04

[58] Field of Search ..... 360/69, 77.02-77.11, 360/78.04-78.14, 75, 40, 51, 97.01, 98.01, 98.02; 364/200

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Primary Examiner—Aristotelis M. Psitos

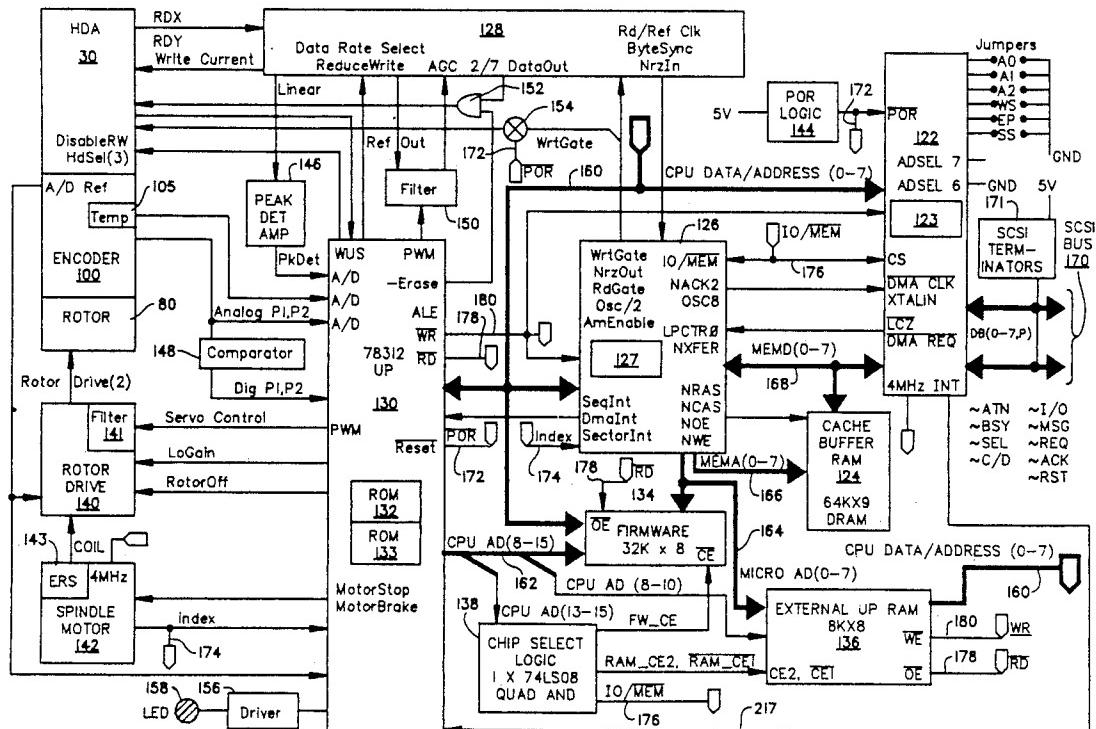
Assistant Examiner—Steven R. Garland

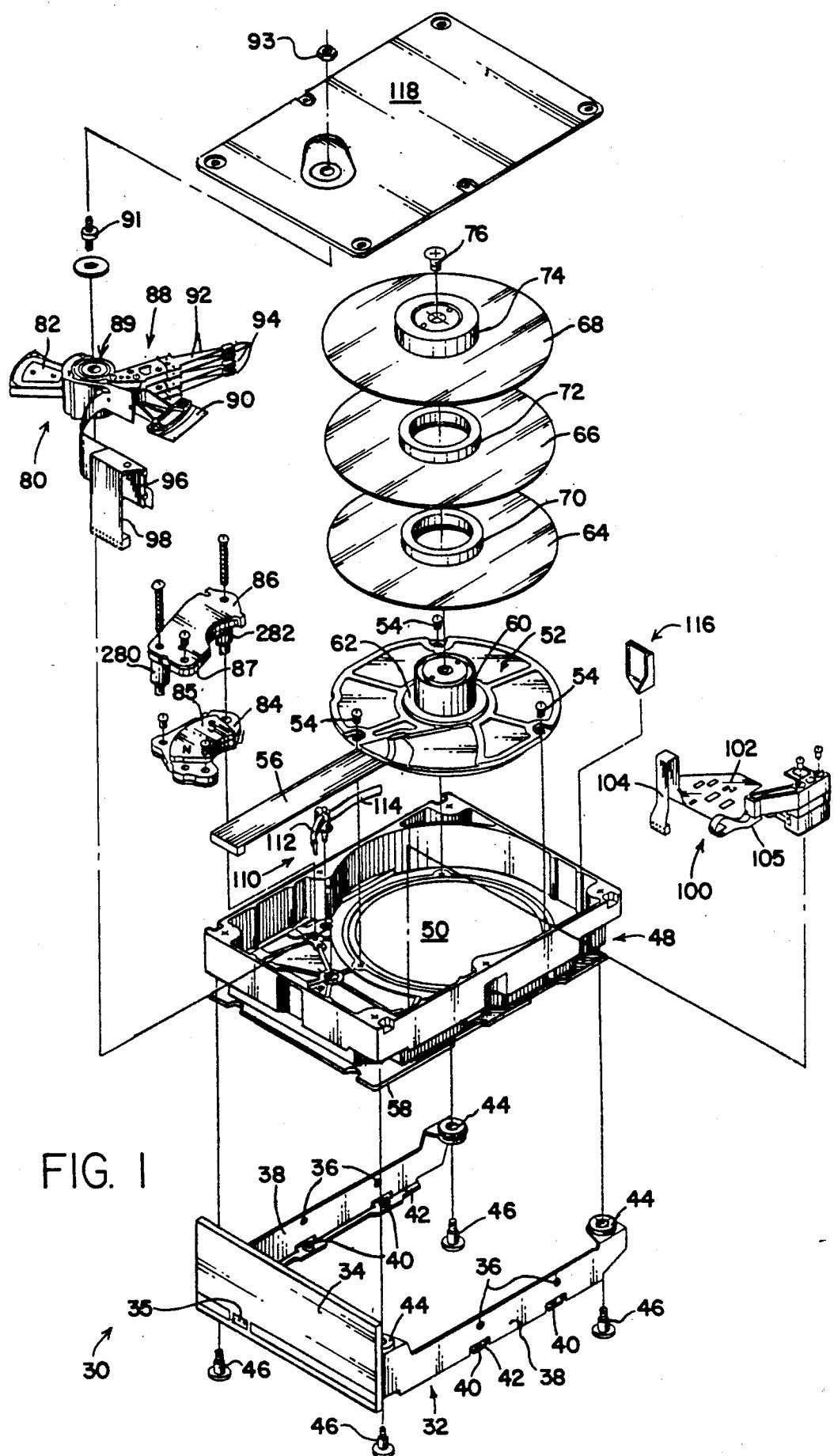
Attorney, Agent, or Firm—David B. Harrison

[57] ABSTRACT

A micro-Winchester disk drive subsystem includes a data block sequencer, cache memory and interface for a host computing machine. The drive includes a base and a plurality of non-removable directly rotated disks forming data storage surfaces. A balanced rotary head transducer actuator is mounted to the base for a plurality of data transducer heads among a multiplicity of concentric data tracks formed on each data storage surface of each of the disks. The track following servo system includes a position encoder coupled between the actuator structure and the base, prerecorded data track centerline information at a radially outermost region and at a radially innermost region of each data surface, and a temperature sensor for sensing temperature of the base at the vicinity of the position encoder. An actuator driver circuit is connected to supply electrical driving current to the actuator structure; and, a single, time divided multi-tasked digital including an analog to digital converter is connected to receive the position information from the position encoder, centerline information from the disk surfaces read by the data transducer and temperature sensed by the temperature sensor during a calibration operation in one phase of its operational cycle, and other phase being devoted to supervision data block handling functions of disk drive data block sequencer cache memory and interface. During track following operations, centerline information is derived from information obtained in the calibrate operation. The temperature sensor is periodically checked and recalibration is carried out when drive temperature changes.

22 Claims, 10 Drawing Sheets





**FIG. I**

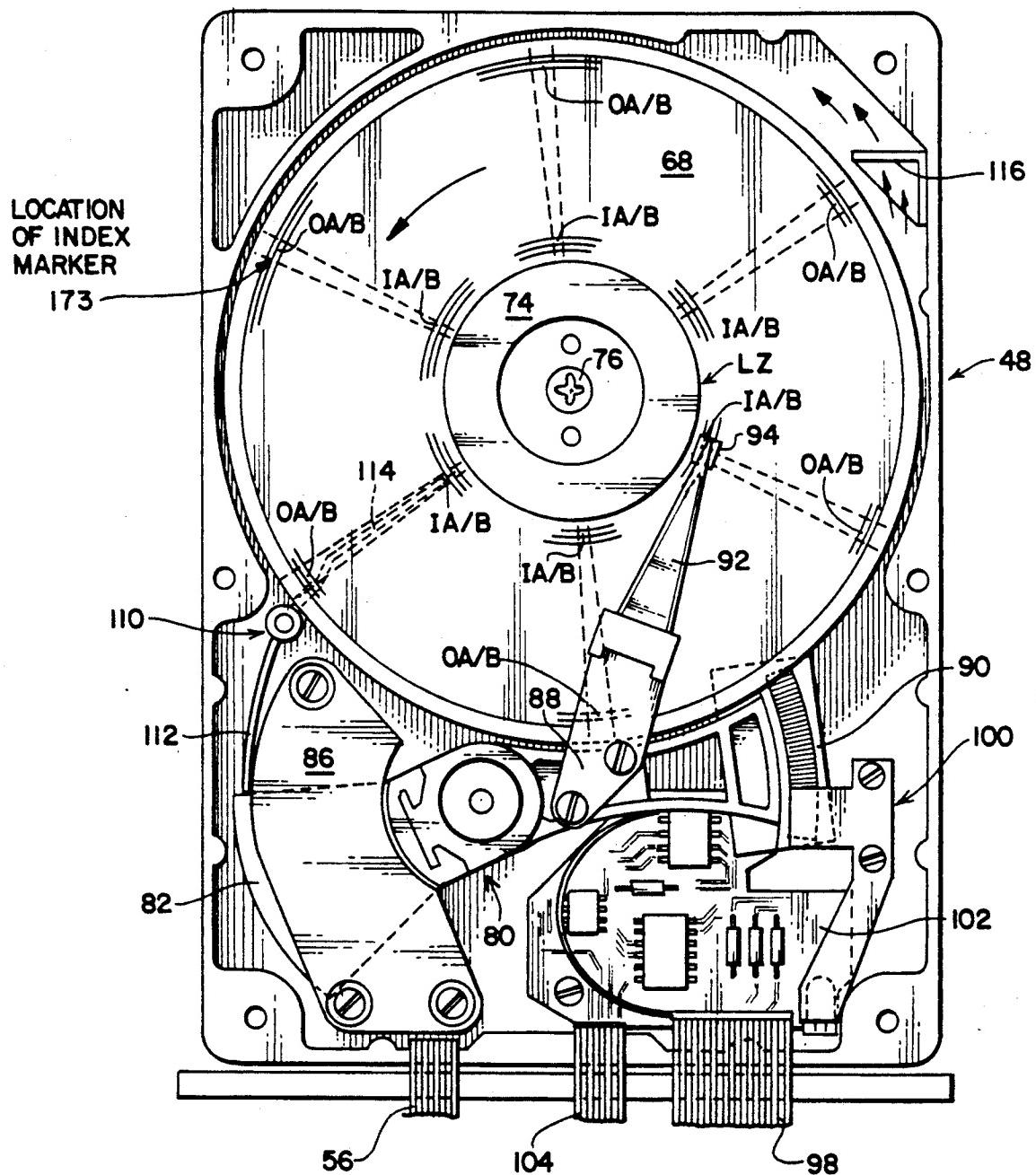
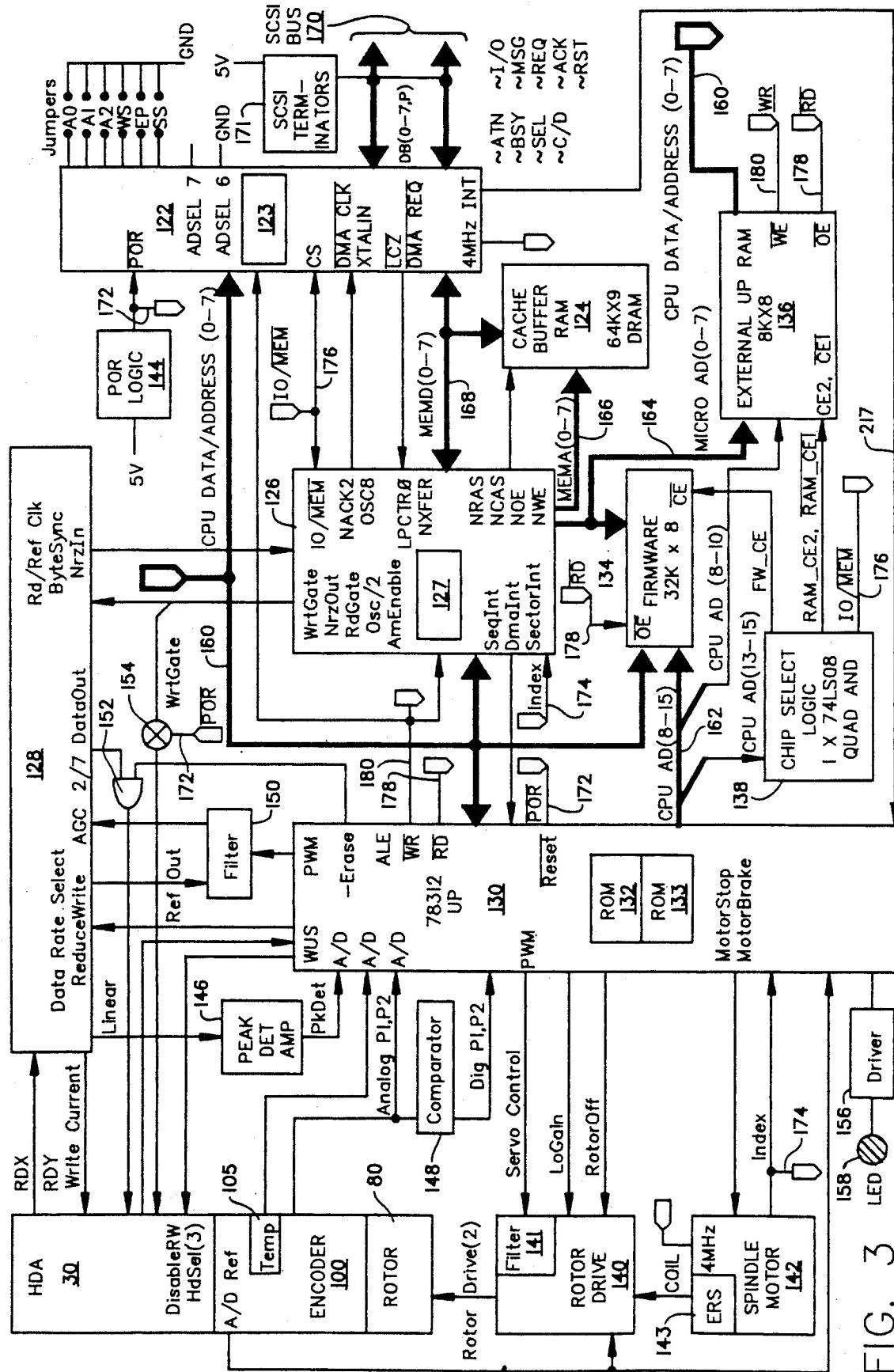


FIG. 2



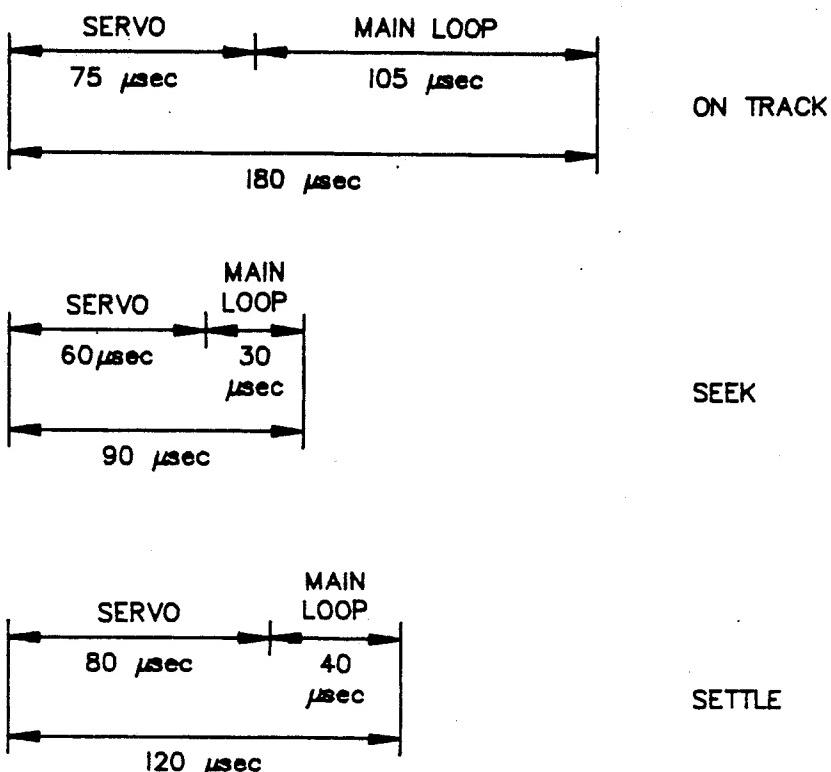


FIG. 4

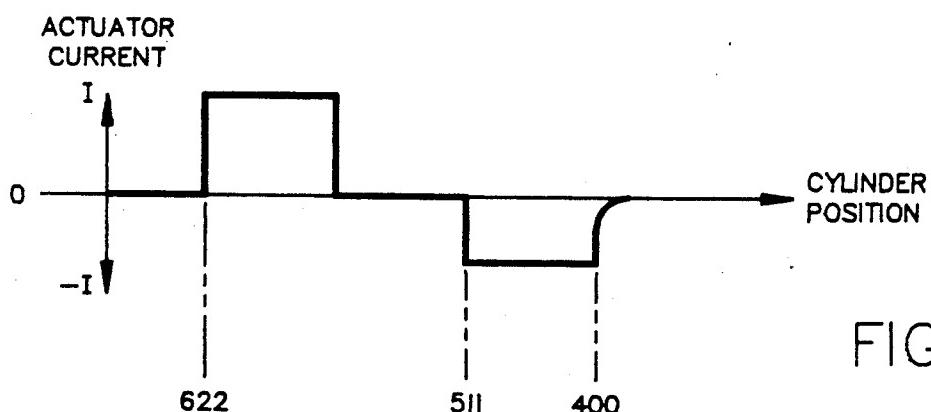


FIG. 6a

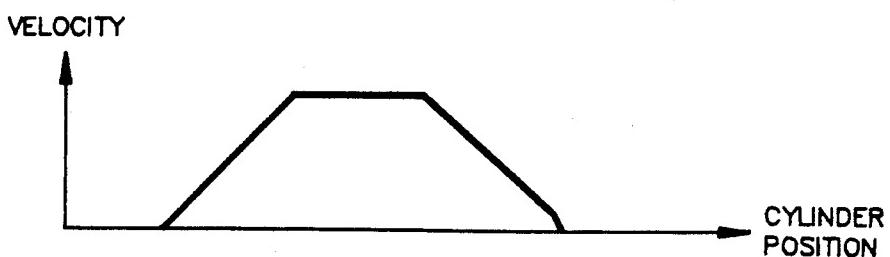
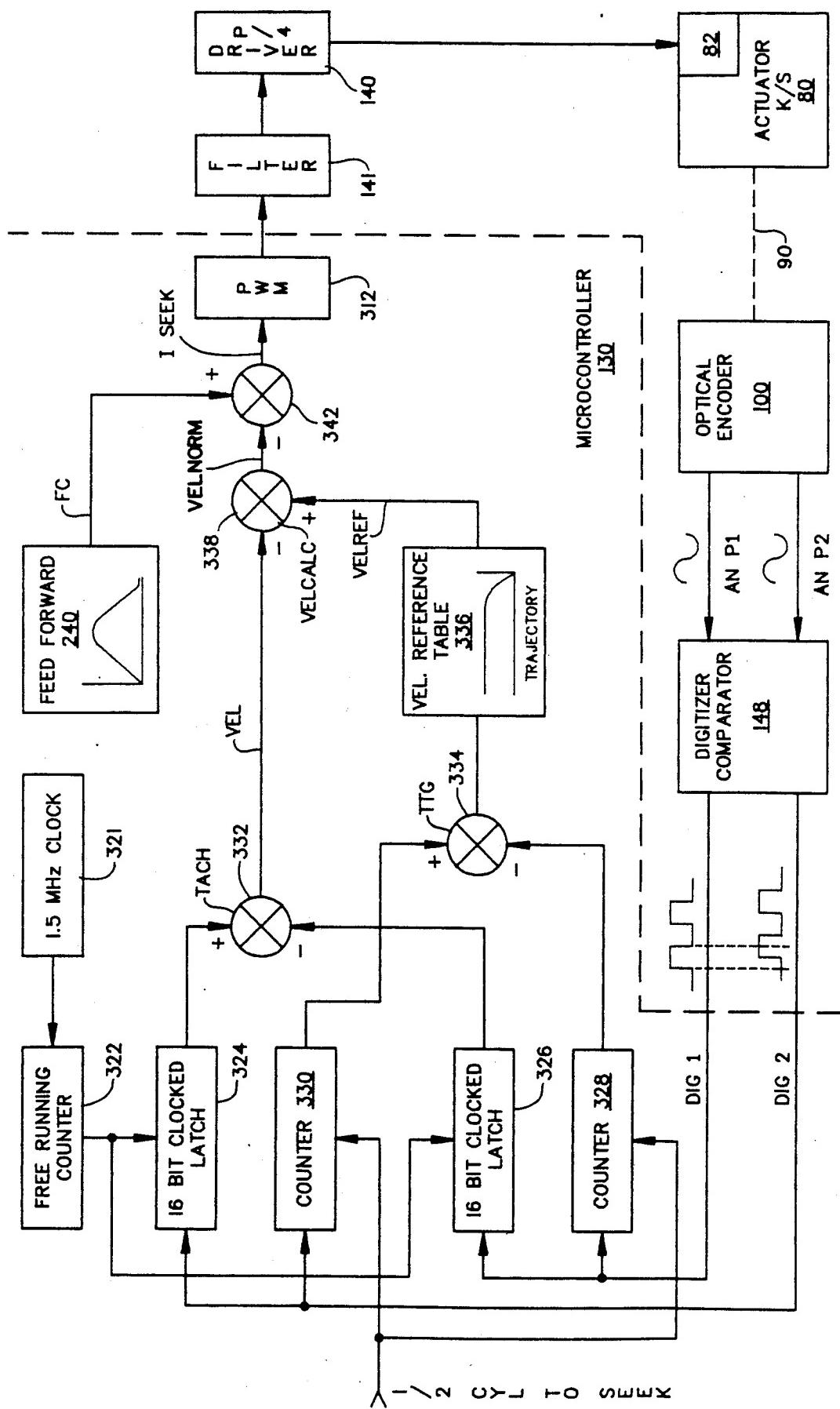
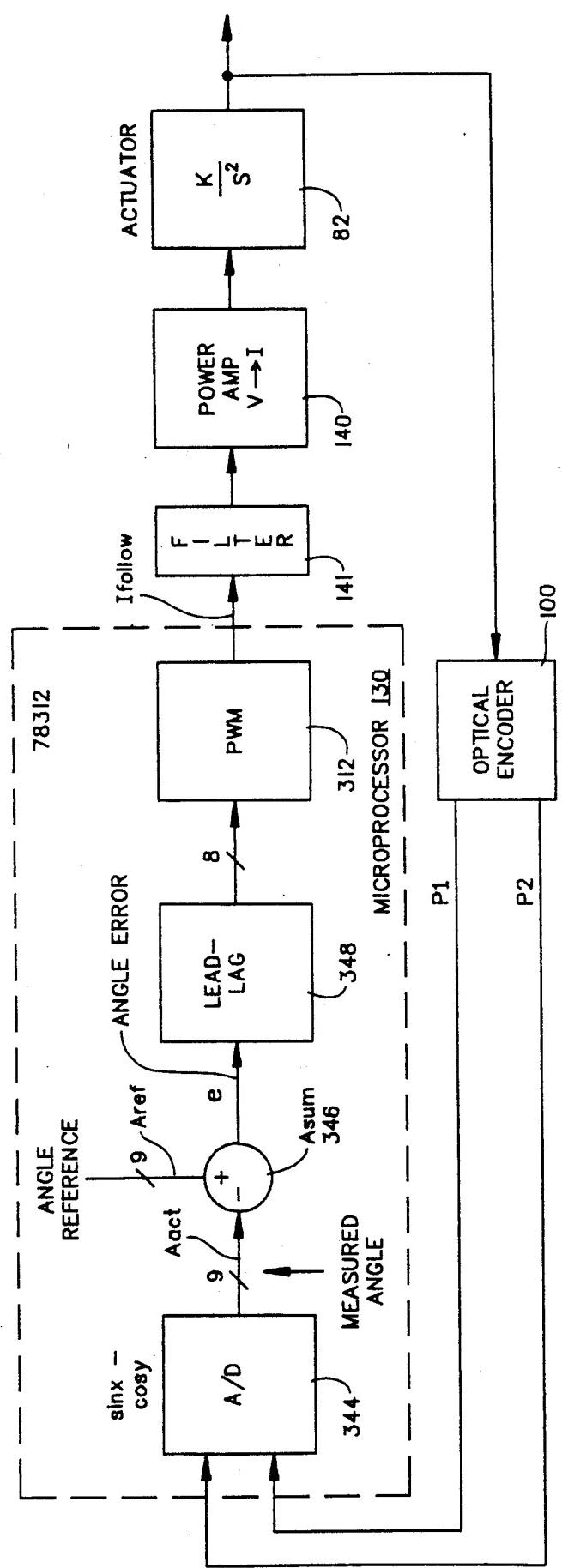


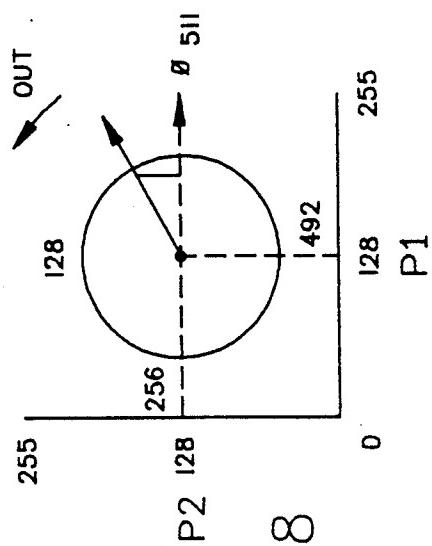
FIG. 6b



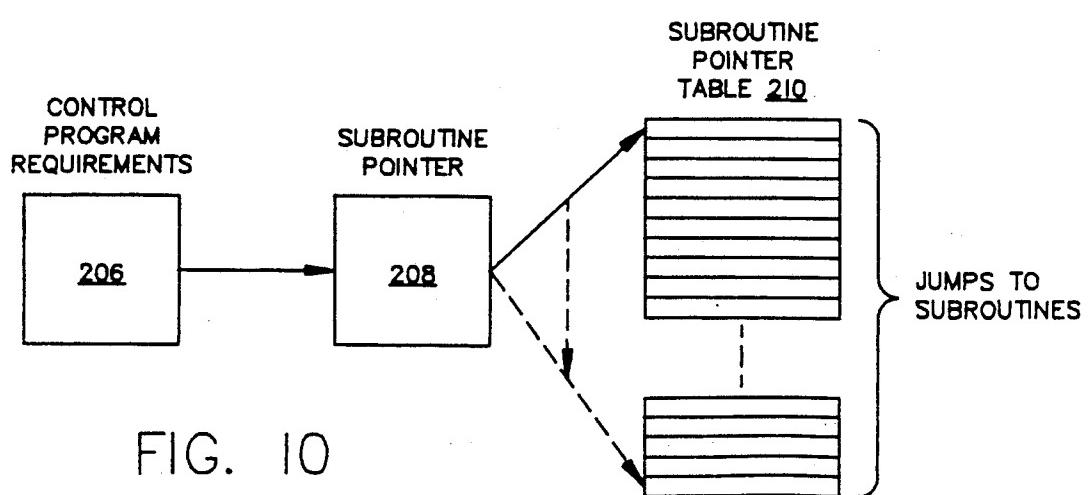
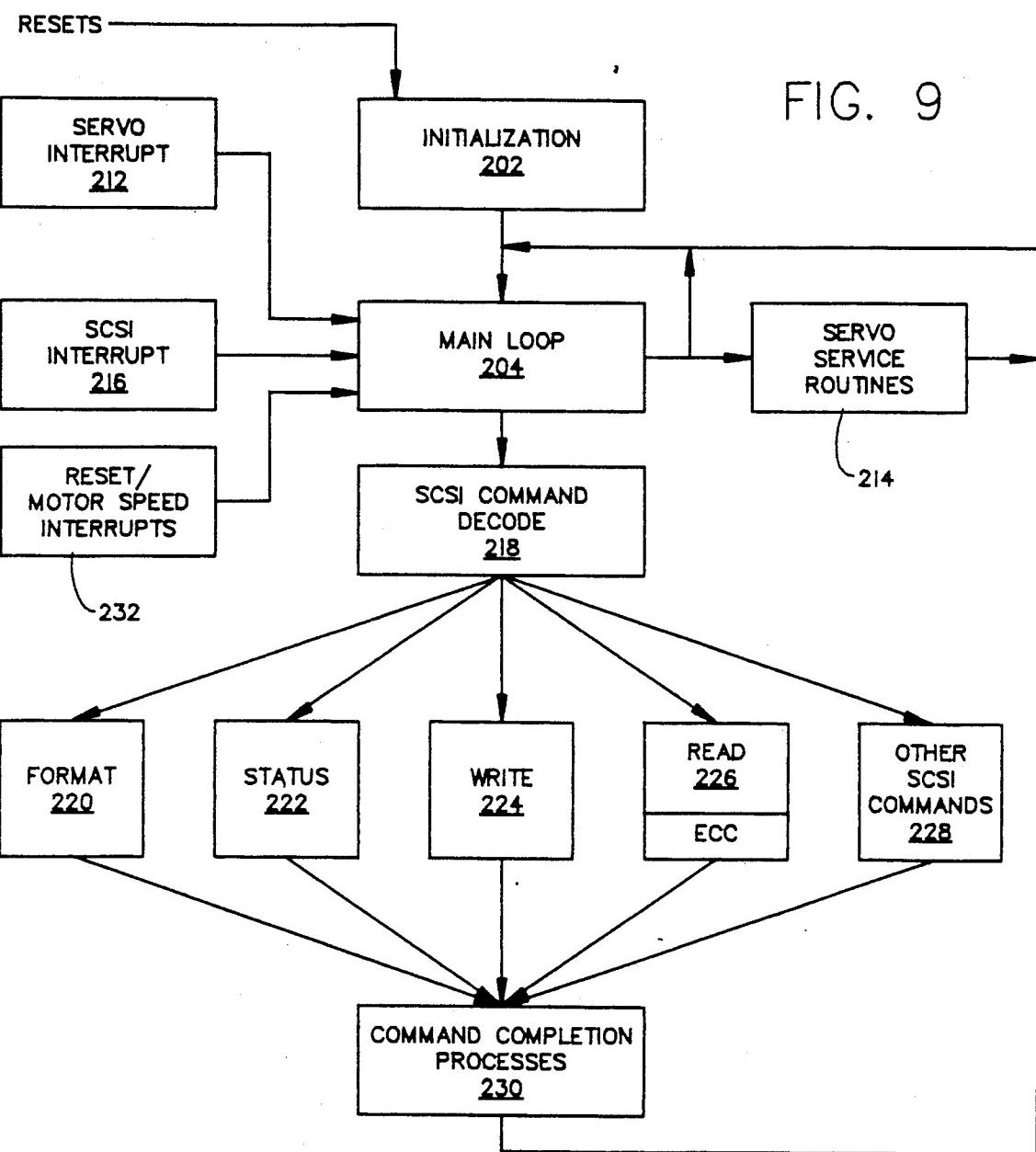


**TRACK FOLLOWING SERVO  
BLOCK DIAGRAM**

FIG. 7



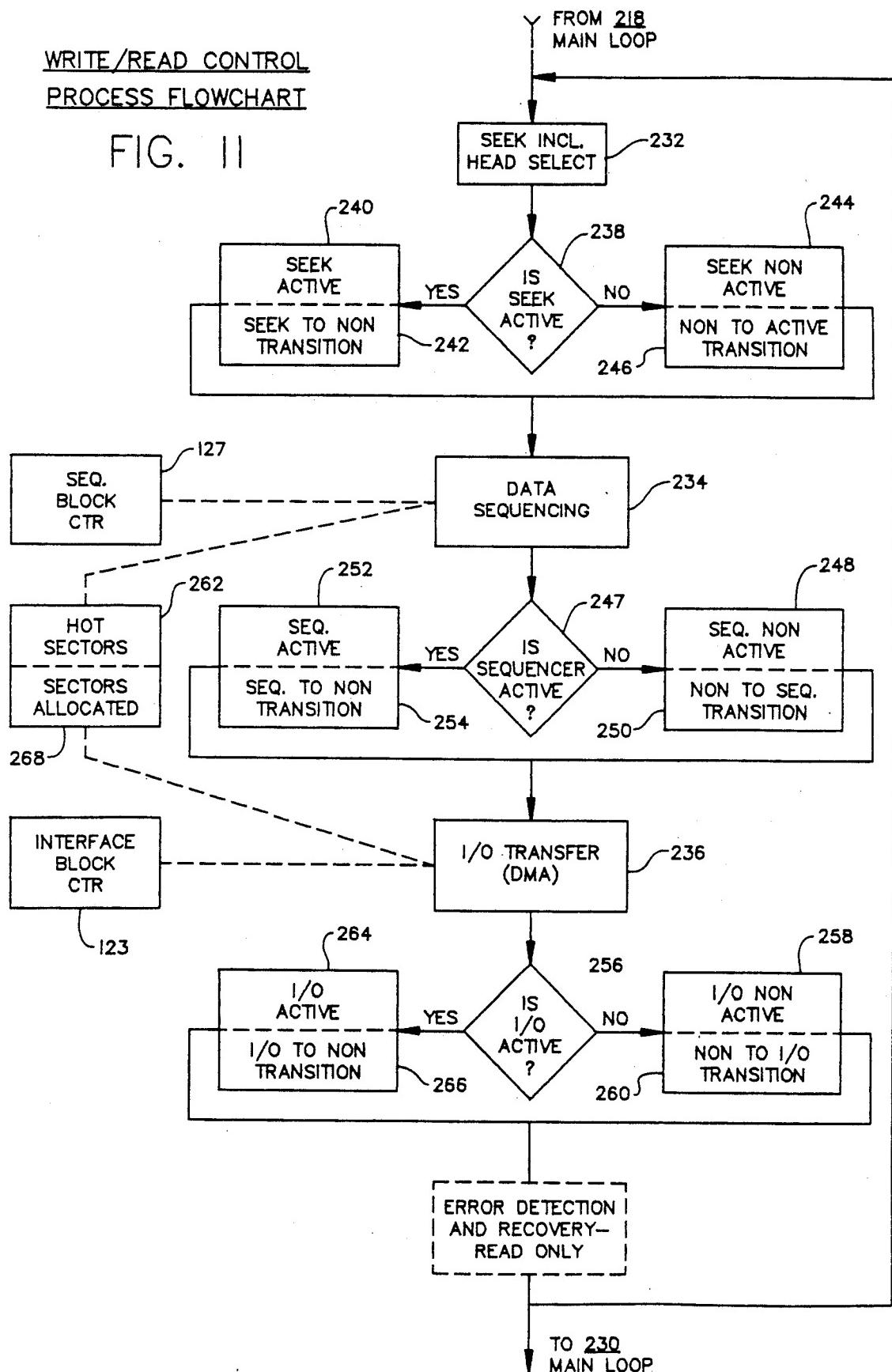
255      128      255  
P2      128      P1



## WRITE/READ CONTROL

### PROCESS FLOWCHART

## FIG. II



## SERVO TRACK FORMAT

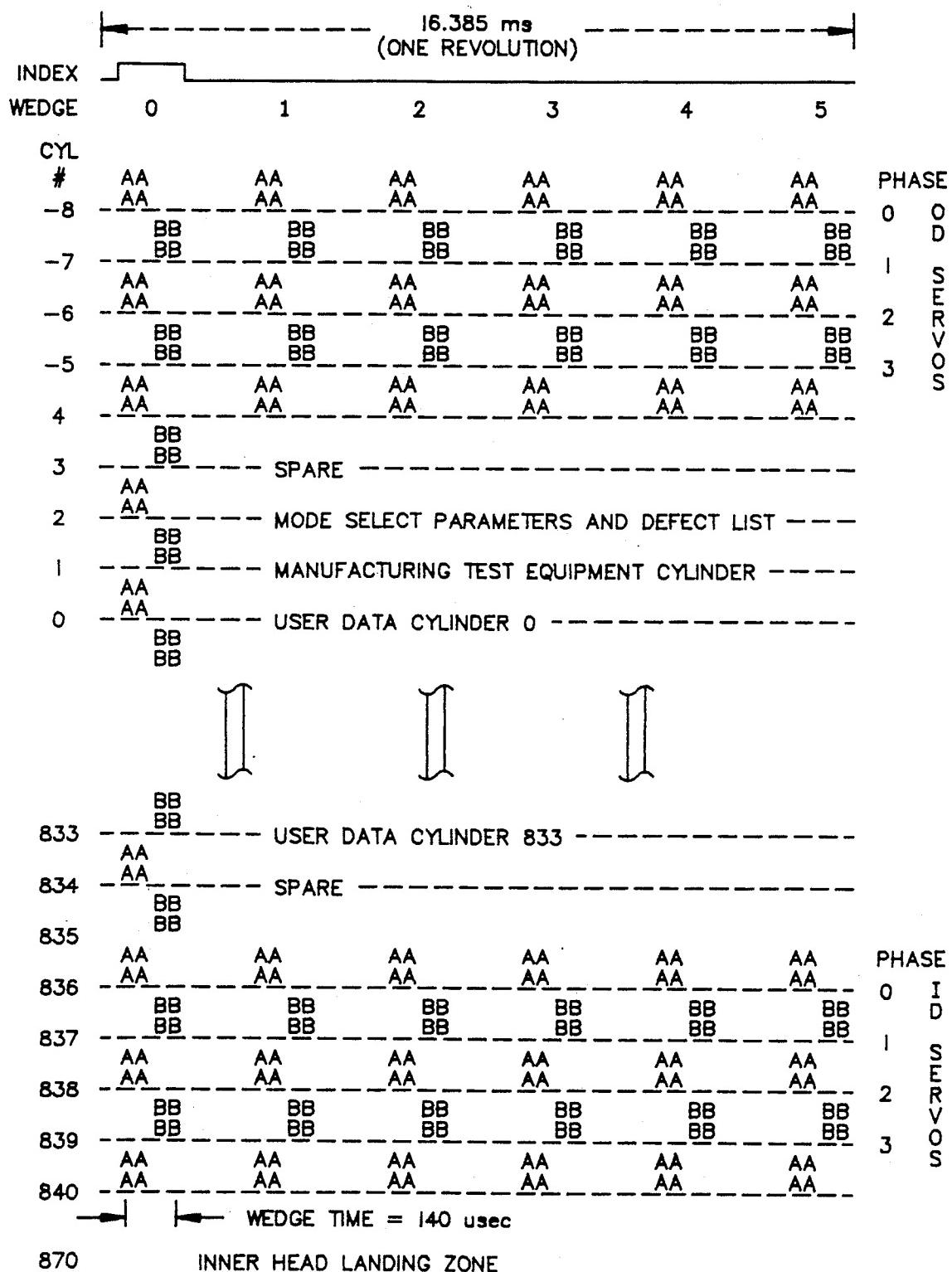


FIG. 12

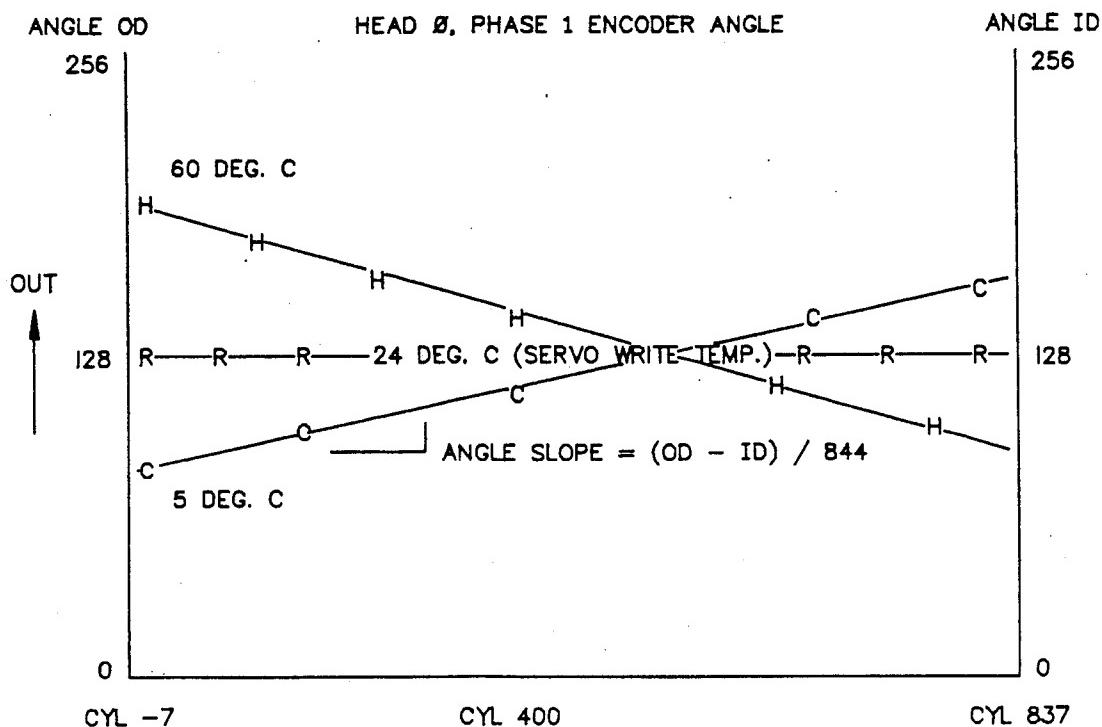


FIG. 13

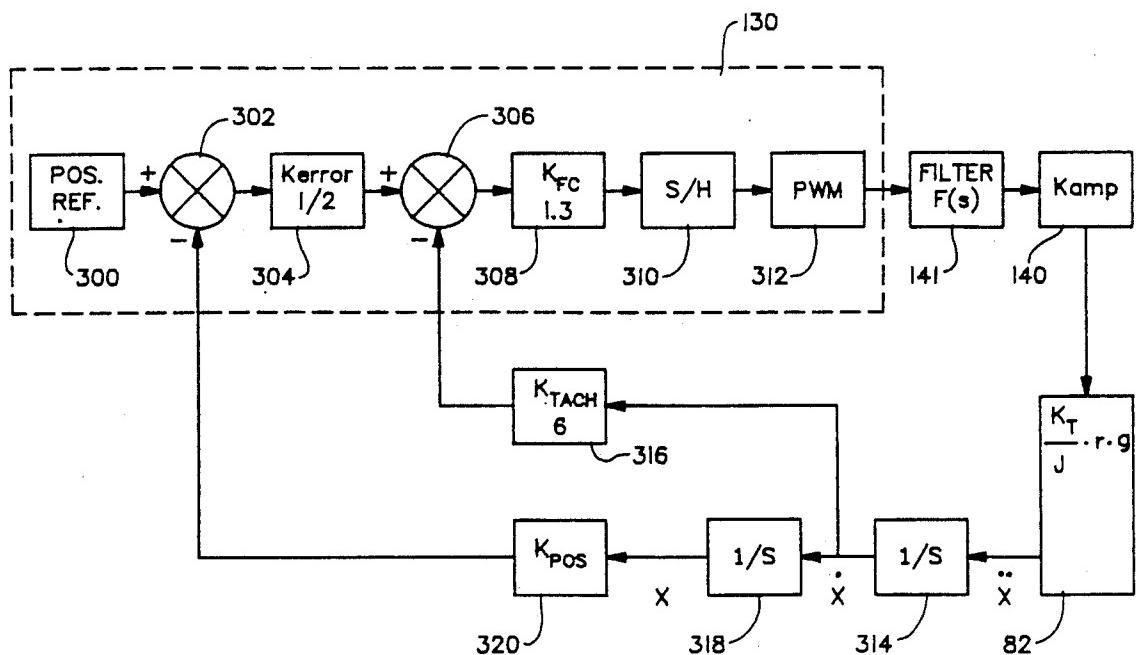


FIG. 14

## HIGH PERFORMANCE, HIGH CAPACITY MICRO-WINCHESTER DISK DRIVE

### Field of the Invention

The present invention relates to data mass storage devices for attachment to computing systems for storage and random access retrieval of vast quantities of data. More particularly, the present invention relates to a low cost, high performance, high capacity micro-Winchester disk drive which combines a number of features to provide greater areal data storage density and shorter average access time in a very small form factor.

### BACKGROUND OF THE INVENTION

The trend toward miniaturization of electronic circuitry and equipment is well documented in the art. In the field of non-removable media rotating disk data storage devices, usually called "disk drives", this trend has been followed, with a definite correlation between the size of floppy disk drives and fixed disk drives. Thus, eight inch diameter floppy disk drives were followed by eight inch diameter Winchester disk drives, see for example the present assignee's U.S. Pat. No. RE 32,075, as an example of a higher capacity, lower cost fixed disk drive. Five and one quarter inch diameter "mini-floppy" disk drives were followed by five and one quarter inch Winchester disk drives, see for example, the assignee's U.S. Pat. No. 4,639,798 which depicts a five and one quarter inch diameter Winchester disk drive as the preferred embodiment (but teaches applicability of the principles disclosed therein to "systems employing either larger or smaller storage disks").

With the introduction of three and one half inch diameter "micro-floppy" disk drives by Sony Corporation, the well developed design trend to follow the floppy disk drive exterior form factor with a corresponding form factor for a Winchester disk drive occurred as an obvious development, see for example, the Rodime PLC U.S. Pat. No. 4,568,988, for a description of a 10 Megabyte micro-Winchester disk drive employing a stepping motor driven head positioner.

As was true about floppy disk drives before them, most early "floppy" form factor Winchester disk drives employed step motor driven head positioning actuators. Such motors intrinsically provided magnetic detents which were used to define the boundaries of each concentric data track followed by the data transducer slider which flew upon an air bearing very close to the data surface. The foregoing referenced disk drive disclosures of the prior art therefore followed a low level computer interface convention as had been first employed with floppy disk drives, where a disk drive controller of the host computer commanded track seek operations at the drive by delivering a stream of stepping pulses to the disk drive, and simultaneously by indicating to the disk drive the direction of stepping, whether toward or away from the periphery of the data storage disks. In the case of eight inch disk Winchester disk drives, the de facto interface standard quickly became the Shugart Associates' SA 1000 interface. In the case of the five and one quarter (and later the three and one half) inch diameter Winchester disk drives, the interface convention became known as the Seagate Technology ST-506 interface (later called the ST-412 interface).

One recognized drawback of open-loop stepping motor positioners has been the relative slowness of such motors and the limited precision thereof. Average track

access times of e.g. 65 milliseconds has been typical of recent microWinchester disk drives employing stepping motor actuators; and, open-loop, step motor precision has been limited to about 600 tracks per inch.

Quasi-closed-loop optical encoder based positioning systems have also been proposed in the prior art. Those systems typically employed voice coil actuators, either linear or rotary, to which a moving scale was attached. The scale moved between a fixed light source and a fixed photodetector array in a manner that generated quadrature position signals. The optical encoder provided track position information. Centerline information was read from a single sector servo area on the servo surface which was hidden or data masked from the controller by lying between an internal index marking signal and a delayed interface index signal. This approach enabled track densities greater than were achieved with the open loop stepper motor positioner approaches while remaining a low cost alternative and without loss of compatibility with the open loop step motor based SA1000 (8 inch) and ST 412 (5 1/4 inch) industry standard interfaces. Examples of such approaches are to be found in the assignee's U.S. Pat. No. 32,075, U.S. Pat. No. 4,419,701 and 4,639,798.

Large system disk drives having a higher level interface, considerably greater data storage capacity and much faster average access times were also known in the prior art. Such interfaces were typically either ESDI, PC-AT or SCSI, and enabled disk drives to be connected directly to computer buses from which command and status words were received and sent, together with blocks of data to be stored or retrieved. High performance has usually required closed loop positioning systems employing voice coil actuators and at least one disk surface devoted entirely to servo information. This information is typically written on servo tracks which are followed by a read-only servo transducer. The overhead cost of the servo surface itself and of the servo writer required to write the servo surface, together with the costs of the readonly servo transducer and related servo channel electronics has rendered the servo surface approach more costly than the step motor detent, or quasi-closed-loop optical encoder based positioning schemes.

One example of a higher capacity disk drive employing a separate servo surface for use with a track following servo loop and an optical encoder with digitized outputs in quadrature for track seeking and for microstepping during track settling is set forth in the present assignee's U.S. Pat. No. 4,516,177.

One example of a PC-AT interface, fully integrated fixed disk expansion board employing a quasi-closed-loop, optical encoder positioned, three and one half inch diameter head and disk assembly and fully integrated controller electronics interfacing directly with a personal computer, such as the IBM Personal Computer (tm), is exemplified by the disclosure set forth in the assignee's subsidiary's U.S. Pat. No. 4,639,863.

Recently, the small computer system interface (SCSI) has obtained prominence within the "floppy disk sized" Winchester disk drive marketplace. One further example of a five and one quarter inch diameter, half height, 80 megabyte, SCSI interface Winchester disk drive with on-board high level command processing capability is disclosed in the assignee's U.S. Pat. No. 4,669,004. While this prior architecture worked well, it manifested a number of drawbacks. First, the embedded servo

sector arrangement adversely affected average access time as the rotary actuator had to be slowed in order not to exceed processing time capacity for handling each servo sector during seeking operations. Second, the somewhat cumbersome software organization of this prior architecture, as well as the use of an eight bit microprocessor controller unduly taxed the controller and extended the response time to SCSI interface requests, thereby limiting data throughput rates.

In summary, while all of the assignee's foregoing disk drive patents described technology marking considerable advances in providing low cost, higher capacity Winchester disk drives, certain drawbacks have remained heretofore unsolved. Primarily, these problems have related to limitations of: (a) areal data densities, (b) track densities limited by thermal drift characteristics, (c) average access times, (d) data block throughput, (e) power supply requirements, (f) noise emissions, and (g) prime costs of manufacture.

#### SUMMARY OF THE INVENTION WITH OBJECTS

Therefore, a primary object of the present invention is to overcome the limitations and drawbacks in prior art Winchester disk drives by increasing areal data storage densities, track densities and data block throughput while reducing average access times, power consumption requirements and noise emission of Winchester disk drives without dramatically increasing either the size or the manufacturing costs associated therewith.

A specific object of the present invention is to provide an improved servo/SCSI command data handling method and controller employing a single microprocessor controller structured and programmed in a unique way in order to speed up data throughput rates and access times.

Another specific object of the present invention is to include hardware counters within memory controller and interface controller state machines so that they may be updated by the microprocessor controller to move blocks of data during intervals when the microprocessor is performing head position servo functions.

Yet another specific object of the present invention is to provide a single microprocessor controller for controlling an intelligent interface Winchester disk drive, which microprocessor includes internal read only memory and random access memory, and which also includes external read only memory and random access memory, and wherein the control program is structured so that time-critical program steps and values are stored internally within the microprocessor itself to reduce processing time, thereby improving overall performance of the disk drive, including program update and revision flexibility.

Yet a further specific object of the present invention is to provide a unique track following servo arrangement for initially calibrating and periodically recalibrating the optical position encoder and other elements subject to mechanical/electrical drift or change with temperature upon directly detecting thermal shifts within the disk drive during its operation.

One more specific object of the present invention is to provide a Winchester disk drive within a three and one half inch diameter industry standard "micro-Winchester" form factor which provides a formatted storage capacity of up to eighty megabytes of data storage, an improved SCSI interface command handling capability, an average track access time of less than twenty milli-

seconds, an expected mean time between failures in excess of fifty thousand hours, and a power consumption requirement of about eight watts, without any substantial increase in prime cost over larger sized prior art disk drives.

In accordance with the principles of the present invention, a disk drive subsystem of the present invention comprises a mounting frame, and a head and disk assembly.

The head and disk assembly includes a base which is shock mounted to the frame, at least one data storage disk fixedly journaled to the base and rotated by a direct drive spindle motor, at least one data transducer flyable in close proximity to a data surface of the disk upon an air bearing, and a head select switch and preamplifier. An electromechanical actuator moves the head among data block locations of the data surface. A position transducer and a temperature sensor are also provided.

An electronic circuit board is mounted to the base within the frame and carries circuitry including a host interface circuit for transferring command and status information and data blocks between the subsystem and a host computer to which the subsystem is attached. The circuit board also includes a cache buffer memory connected to the host interface circuit for storing data blocks to be transferred. A direct memory access controller is connected to control addressing of the cache buffer memory. A data sequencer is connected to the cache buffer memory for serializing and deserializing data blocks transferred to and from the disk surface and the cache buffer memory. A data channel circuit is connected between the data sequencer and the head select and preamplifier circuit.

The electronics board also includes a bi-phase task divided single programmed digital microcontroller which, during a first task phase, obtains and executes commands from the host and returns status information to the host, and supervises transfers of blocks of data between the host interface circuit and the data surface, and controls gain compensation of the data channel electronics; and, during a second task phase, controls the electromechanical actuator during track seeking and track following operations from information provided from the position transducer as corrected by prestored calibration information, the digital microcontroller being programmed to obtain the calibration information when power is initially applied to the subsystem and to update the calibration information whenever a thermal shift is sensed by the temperature sensor. The calibration information includes track centerline servo information read from an outermost and an innermost track region of the data surface.

In the present invention, data throughput is increased by providing data block loop counters within the data sequencer and host interface circuit which may be updated by the microcontroller to enable block transfers to continue during second task phase intervals when the microcontroller is supervising servo control of the actuator structure.

Another aspect of the present invention is that the data sequencer and the host interface circuit operate as state machines asynchronously with respect to each other and coordinate their activities by communicating through commonly accessible microcontroller registers denominated "hot sectors" and "sectors allocated".

A further aspect of the present invention is that the calibration routine takes into account the inward seek-

outward seek hysteresis characteristic of the actuator structure.

Also, the actuator coil is designed to counterbalance the in-line rotary actuator structure in order to reduce the counterweight heretofore used and to thereby reduce mass and decrease average access time of the actuator. The actuator coil is preferably integrally molded to the rotary actuator hub with a brass counterweight integrally molded into the center space surrounded by the coil so that the coil assembly counterbalances the mass of the heads and optical encoder scale, while presenting a minimum rotary inertia.

Another aspect of the present invention is the provision of an aerodynamically released shipping latch which is so designed to enable independent assembly and disassembly of the disk stack and rotary actuator structure.

The foregoing and other objects, aspects, advantages and features of the present invention will be more fully understood and appreciated by considering the following detailed description of a preferred embodiment, presented in conjunction with the accompanying drawings.

#### BRIEF DESCRIPTION OF THE DRAWINGS

##### In the Drawings:

FIG. 1 is an exploded isometric view of a head and disk assembly of a micro-Winchester disk drive subsystem incorporating the principles of the present invention.

FIG. 2 is an approximately life size top plan diagrammatic view of an assembled head and disk assembly of the type depicted in exploded view in FIG. 1.

FIG. 3 is an overall electrical system block diagram of the circuitry included within the FIG. 1 micro-Winchester disk drive subsystem.

FIG. 4 is a diagram illustrating division of processing time between servo and controller supervision tasks of the single microprocessor controller of the FIG. 3 subsystem.

FIG. 5 is an architectural model block diagram of the FIG. 3 subsystem operating from velocity information in the track seeking mode during servo time.

FIG. 6A is a graph of a seek mode feed forward prediction waveform generated within the velocity servo loop depicted in FIG. 5.

FIG. 6B is a graph of resultant velocity from the FIG. 6A prediction waveform as normalized by combination with a VELNORM value derived from actual velocity.

FIG. 7 is an architectural model block diagram of the FIG. 3 subsystem operating from position information in the track following mode during servo time.

FIG. 8 is a graph of angular information derived from the optical encoder of the FIG. 3 subsystem operating in the track following mode during servo time.

FIG. 9 is an overview flow diagram of the control programs executed by the single microprocessor controller of the FIG. 3 subsystem.

FIG. 10 is a diagram showing how service routines are pointed to during main loop time of the FIG. 8 flow diagram.

FIG. 11 is flow diagram of READ and WRITE command execution service routines.

FIG. 12 is a servo information budget plan which graphs the placement of A/B servo bursts within each of the inner and outer servo tracks.

FIG. 13 is a graph showing the manner in which the prediction angle for a given head and phase will vary over temperature.

FIG. 14 is a functional block diagram of the FIG. 3 subsystem operating from position information in the angle servo seek mode during servo time.

#### Detailed Description of a Preferred Embodiment

##### Head-Disk Assembly 30, FIGS. 1 & 2

A head and disk assembly 30 of a micro-Winchester disk drive subsystem 10 incorporating principles of the present invention is shown in FIG. 1 and 2. The assembly 30 is similar to the assembly described in U.S. Pat. No. 4,712,146, incorporated by reference, although the present assembly 30, having three disks and an overlying printed circuit board, has a thickness (one and five eighths inch) which is slightly greater than the thickness dimension originally achieved in the two disk head and disk assembly described in the referenced '146 patent.

The assembly 30 includes a metal frame 32 and faceplate 34. A translucent lens 35 attached to the faceplate 34 enables light from an LED activity lamp 158 mounted on a main printed circuit board 58 to be visible at the faceplate 34 when the disk subsystem 10 is active. The frame 32 includes threaded openings 36 on opposite sides 38 and threaded openings 40 extending through bottom flanges 42 of the opposed sides 38. The threaded openings 36 and 40 are conventionally located and sized to enable the subsystem 10 to be mounted within standard micro-floppy/micro-Winchester mounting configurations of a host computing system (not shown) with which the subsystem 10 is to be connected and used. Shock absorbers 44 and bolts 46 are used to secure a formed base 48 to the frame 32 while providing isolation of the base from externally induced shock forces.

The base 48 may be cast or otherwise formed of any suitable formable material, such as aluminum alloy, and it includes a rib-reinforced bottom wall and contoured sidewalls as shown in FIG. 1. A thin aluminum plate cover 118 is attached through a gasket (not shown) to the machined top surfaces of the contoured sidewalls in order to enclose and seal the interior space. Portions of the flex circuit cables pass between the machined top surface and the gasket in order to facilitate connection with the electrical elements within the interior space.

An annular opening 50 is defined in the bottom wall of the base 48. A DC brushless three phase spindle motor 52, rotating at a constant angular velocity, e.g. 3662 RPM, is mounted through a gasket (not shown) in the opening 50 by three screws 54. A thin film conductor cable 56 enables the three stationary windings, the three Hall effect commutation sensors, and a once per revolution index marker Hall effect sensor, of the motor 52 to be plug-in connected to electronic driving circuitry carried on a single printed circuit board 58. The motor 52 includes a spindle hub 60 which includes pre-loaded spindle bearings and a ferrofluidic seal to prevent ambient air from entering the enclosed interior space via the spindle. The spindle hub 60 includes an integrally formed lower flange 62.

Preferably, three data storage disks 64, 66 and 68 are mounted to the spindle hub 60. The disks 64, 66 and 68 are typically formed of aluminum alloy material sputter coated with a thin magnetic metal film data storage media. The film media is coated with a carbon overcoat which prevents head and media wear within an inner landing zone LZ where the head touches down on each

data surface whenever the spindle motor 52 has stopped rotation. The metal film coating provides a suitable data storage media for storage of data in a multiplicity of concentric data tracks formed on each major surface of each disk.

A track density of 1000 tracks per inch is presently achieved in the subsystem 10, although significantly higher track densities, such as 1300 tracks per inch are clearly feasible. With six heads and 834 data cylinder locations per actuator position or "cylinder" location, 10 each cylinder having six data tracks, and with a 2,7 run length limited recording density of 22,055 bits per inch, an overall data storage capacity of 80,886,080 bytes formatted is achieved by the subsystem 10. In a reduced storage capacity subsystem including two disks (three data surfaces) and three heads, a data storage capacity of 40 megabytes formatted is achieved. The one unused data surface may be one determined to contain excessive media defects during the manufacturing process. In this way the other, useful surface is used, thereby 20 achieving further economies in manufacturing. Average power consumption of the subsystem 10 including the spindle motor 52 is 8 watts.

The hub flange 62, spacers 70 and 72, and a top securing disk 74, space apart the disks 64, 66 and 68 about the 25 rotating spindle hub 60. A screw 76 clamps the disks 64, 66 and 68 to the hub 60.

The circuit board 58 is mounted by screws to the underside of the base 48. An insulating shield (not shown) consisting of a layer of plastic film laminated to 30 a layer of copper foil is sandwiched between the underside of the circuit board 58 and the outer surface of the metal base 48, with the copper side facing the base 48. The plastic film layer prevents the electrical circuit paths on the board 58 from shorting to or through the 35 base 48. The copper layer serves to shield the data transducer heads 94 from radiated electromagnetic noise generated on the board 58.

A rotary actuator structure 80 is journaled to the base 48 and to the cover plate 118 for mechanical rigidity. The structure 80 includes a moveable single phase coil 82 rotatably disposed in a magnetic field gap formed between two ferromagnetic flux return magnet plates, a bottom plate 84 and a top plate 86. The plates 84 and 86 may each be constructed of several thin plates which are sufficiently thin to be stamped out during the manufacturing process, yet thick enough when stacked together to handle and contain the magnetic return flux. Two high flux density neodymium alloy permanent magnets 85 and 87 define adjacent, alternating north-/south poles on the opposed faces thereof and are bonded to their respective flux return plates 84 and 86. The magnets 85 and 87 provide the flux in the gap between the two plates 84 and 86. Two rubber cylinder crash stops 280 and 282 are mounted by posts and screws which mount the two plates 84 and 86 together in a spaced apart relationship defining a magnetic gap in which a moving coil 82 is able to move along a locus of limited angular displacement, the limit thereof being established by the thickness of the coil 82 and the distance between the crash stops 280 and 282.

A hub and disk spindle assembly 89 includes pre-loaded bearings having ferrofluidic seals. The bearings are journaled to a fixed shaft pressed into the base. A screw 91 and nut 93 secure the hub to the top cover 118.

A transducer arm assembly 88 includes a moving glass scale 90 and six in-line Whitney flexures 92 which secure six mini-composite data transducer head struc-

tures 94 which fly in very close proximity (seven micro-inches, for example) to the data surfaces via an air bearing effect. A thin metallic foil sheet is bonded to each of the flexures 92 with a viscoelastic damping adhesive in 5 order to dampen mechanical resonances.

The arm assembly 88 is designed such that its mass center is at the center of the hub 89, by virtue of the presence of an integrally molded brass counterweight in the central space surrounded by the windings of the coil 82.

The range of angular displacement of the actuator structure is sufficient to define 834 cylinder locations. With the six heads 94 and 834 cylinder locations, 5004 data tracks are defined on the data surfaces. Fourteen extra cylinders are provided in a radially outermost region, and extra room is provided in a radially innermost region inside of track number 839 comprising a landing zone LZ, as graphed in the track budget aspect of FIG. 12.

A flexible printed circuit substrate 96 carries a head selector/read-write preamplifier integrated circuit, such as type SSI 501. Power and data connections are made to the main printed circuit substrate 96 via an extension portion 98 which plugs into a read channel circuit 128 carried on the main printed circuit substrate 58.

An optical encoder assembly 100 is of the type described in U.S. Pat. No. 4,703,176, incorporated by reference; and, it cooperates with the moving scale 90 to provide two phase position signals P1 and P2 in quadrature relation (90 degree phase shift between signals i.e. sine and cosine signals). There are four data track locations defined by a complete optical cycle of the moving scale 90 relative to the photodetector array of the assembly 100. The moving scale 90 and the reticle of the photodetector array of the assembly 100 are configured to have a resolution of 1000 tracks per inch.

The circuitry of the optical encoder assembly 100 is carried on a thin polyimide film substrate 102 which 40 includes a connecting cable portion 104 which plugs into the printed circuit board 58. Lead-lag phase trim and symmetry adjustments are made at the factory in accordance with the techniques taught in the assignee's U.S. Pat. Nos. 4,647,769 and 4,661,696, incorporated by reference. Preferably the scale 90 and disks 64, 66, and 68 are formed of materials having linear coefficients of thermal expansion.

A temperature sensing thermistor 105 is also carried on the thin polyimide film substrate 102; the thermistor 50 105 makes direct thermal contact with the interior bottom wall of the base 48 at the vicinity of the optical encoder assembly 100 in order to sense temperature thereat. The thermistor 105 is periodically scanned by a microcontroller 130 which determines whether any 55 change in temperature at the base 48 has occurred. When a thermal shift is noted, the microcontroller 130 causes the optical encoder assembly 100 and other thermally sensitive elements to become electronically recalibrated by reference to servo information read from the surfaces of the disks 64, 66 and 68 and read channel gain recalibration in a manner explained in greater detail hereinafter.

A spring-loaded aerodynamic actuator latch release mechanism 110 similar to one described in U.S. Pat. No. 4,647,997, incorporated by reference, is also journaled to the base 48. In this particular embodiment of air vane latching mechanism, a latch portion 112 directly engages a side of the moving coil 82 as best seen in FIG.

2. A vane portion 114 is disposed between the disks 64 and 66 as shown in broken line view in FIG. 2. With the particular embodiment of air vane mechanism 110 as depicted in FIGS. 1 and 2, it is possible to remove the disk stack when the vane portion 114 is moved to a position against the adjacent sidewall of the base casting 48; and it is also possible to remove the rotary actuator structure 80 from its journal when the latch portion 112 is moved to a position against the same adjacent sidewall.

When properly commutated DC power phases are applied to the three phase brushless spindle motor 52 and the disks 64, 66 and 68 are rotating at operational speed, airflow generated by disk rotation overcomes the bias force of the loading spring and deflects the vane portion 114. The latch portion 112 then moves free of the moving coil 82 and frees the actuator structure 80 so that it may rotate throughout its limited range of angular displacement.

Whenever DC power is removed from the spindle motor 52 and it begins to spin down, an electronic return spring circuit 143 senses this power-down condition and converts the spindle motor 52 into a generator, so that rotational energy stored in the rotating disk stack is converted to electricity and applied to cause the rotor coil 82 to move the actuator assembly to place the heads 94 over the landing zone LZ. When the disks slow down sufficiently, airflow is insufficient to deflect the vane portion 114, and the latch portion reengages the coil 82, thereby locking the actuator structure 80 as the heads 94 land at the landing zone LZ. The actuator structure 80 thereafter remains locked until the disks once again begin to spin up to operating angular velocity and the force of the bias spring is overcome.

A 0.3 micron micropore dust filter structure 116 is mounted in one corner of the base 48 in the path of airflow (shown by arrows in FIG. 2) generated by counterclockwise disk rotation as viewed from the top of the assembly 30 with the cover 118 removed. Any 40 dust or particulate matter otherwise present or becoming loose within the enclosed interior space of the head and disk assembly 30 becomes trapped in the filter 116. A 0.3 micron breather filter (not shown) is provided through the thin aluminum plate cover 118 just above the disk spindle hub 74 where internal air pressure is at its lowest. As is well understood by those skilled in the art, the head and disk assembly 30 is actually assembled in a clean room or clean tunnel environment providing a Class 100 purified air environment in order to minimize particulate contamination of the interior of the assembly, so that the heads 94 do not strike particles as they fly so very close to the magnetic data storage surfaces.

#### Servo Information, FIG. 2

Servo information, preferably in the form of radially offset, time-sequential A/B servo bursts in servo sectors within inner and outer tracks in a manner described in the referenced U.S. Pat. No. RE 32,075, is prerecorded on each data storage surface. A servo information budget plan is depicted in FIG. 12 which graphs the placement of A/B servo bursts within each of the inner and outer servo tracks. The A/B bursts are recorded at the factory by the data transducer heads of the disk drive 65 subsystem 10, based upon optimal track spacing information derived from an optical position encoder 100, discussed hereinafter.

In the subsystem 10, servo information labelled OA/B is recorded at the factory in a single sector on each surface in four outer cylinder locations -8, -7, -6 and -5 (it being understood that cylinder zero, the first 5 data track directly available to the host system is e.g. the fourteenth physical track from an outer crash stop). Servo information labelled IA/B is also recorded in a single sector on each surface in four innermost cylinder locations, cylinders 836, 837, 838 and 839. Such servo 10 information OA/B and IA/B is available to be read by the transducers 94 during optical encoder servo calibrate operations, to be explained in greater detail hereinafter. The use of servo information in outermost and innermost data tracks with linear spread of difference 15 during an initialization calibration process is disclosed in the referenced U.S. Pat. No. RE 32,075.

As shown in FIG. 2, there are six circumferentially staggered sectors, one of which is associated with each data surface. The sectors begin with a spindle index 20 marker 173 and are circumferentially offset for each data surface, so that servo information may be read from every data surface within a particular data cylinder during a single revolution of the disk stack, merely by switching transducer heads after each servo sector 25 has passed by and the servo information therein peak-sampled, converted to digital information and then held digitally in microcontroller register locations.

#### Control Electronics 120, FIG. 3

30 Circuit elements comprising subsystem control electronics 120 are principally assembled and interconnected on the main printed circuit board 58. As illustrated in the block diagram of FIG. 3, in the subsystem 10 there are six main subparts of the control electronics 120: a host (e.g. SCSI) bus interface circuit 122 having an internal input output data block loop counter 123; a 64 KByte cache buffer dynamic random access memory array 124; a combined data sequencer/DMA controller circuit 126 having an internal disk data block loop counter 127; a data synchronizer/encoder-decoder data channel circuit 128; a single supervisory microcontroller 130 having internal read only memory 132 and random access memory 133, external read only memory 134, external random access memory 136, chip select logic 138, and analog rotor driver circuitry 140 having an internal pulse width modulation to analog converter and filter 141; and, a spindle motor commutation controller and driver circuit 142 including the electronic return spring circuit 143.

50 The external read only memory 134 and external random access memory 136 are provided respectively to hold major portions of the control program and live time variables. The internal read only memory 132 includes time critical interrupt service routines such as

55 servo interrupt service, seek interrupt service, Cache buffer service, and those of the command overhead service routines which must be executed very quickly. Access time to internal memory is one half of the access time to external memory. The internal random access 60 memory 133 receives blocks of variables that are specifically selected by a particular task. For example, calibration values appropriate to a particular seek destination would be transferred as a block from the external RAM 136 to the internal RAM 133. These values would be calibration values corresponding to a particular head and phase of the optical encoder, such as head gain co-efficient and slope, optical phase offset and slope, etc.

Other circuits of the subsystem 10 include: a power on reset logic circuit 144, a peak detector amplifier circuit 146, an analog to digital comparator circuit 148, an external pulse width modulation to analog converter and filter circuit 150, an AND erase gate 152, a summing junction 154, an activity lamp driver circuit 156 and LED activity lamp 158.

A CPU eight bit cycle-multiplexed data/address bus 160 interconnects the microcontroller 130 with the SCSI bus interface circuit 122, the data sequencer/DMA controller circuit 126; the external firmware ROM 134 and the external controller RAM 136. The bus 160 carries eight bits of data during read and write cycles of the microcontroller 130 and carries the low order eight bits of address information (A0-A7) during address latch enable cycles thereof. A CPU high order address bus 162 carries the high order eight bits of address information (A8-A15) during read and write cycles of the microcontroller 130; this bus 162 extends to the firmware ROM 134, external RAM 136 and the chip select logic 138. A microchannel address bus 164 carries eight bits of address information from the data sequencer/DMA controller circuit 126 to the external firmware ROM 134 and to the external RAM 136. A DMA address bus 166 extends from the data sequencer/DMA controller circuit 126 to the cache buffer RAM 124. A DMA data bus 168 extends between the SCSI bus interface circuit 122, cache buffer RAM 124, and data sequencer/DMA controller circuit 126. A SCSI bus 170 connects the SCSI bus interface circuit 122 to a host computer (not shown) having a conventional SCSI port. A SCSI termination resistor network 171 sets the lines of the SCSI bus 170 to a logic high level in absence of logical activity at the circuit 122. The internal counters 123 and 127 of the SCSI interface circuit 122 and of the data sequencer/DMA controller circuit 127 are directly addressable by the microcontroller 130.

A power on reset signal line 172 distributes a power on reset signal generated by the power on reset logic 144 to the SCSI bus interface circuit 122, HDA circuitry 96 via the junction 154, and microcontroller 130 so as to initiate poweron initialization of the subsystem 10. A disk once-perrevolution index marker signal 173 (FIG. 2) generated internally within the spindle motor 52 is processed and shaped by the spindle motor processor circuit 142 and distributed on an index line 174 to the data sequencer/DMA controller circuit 126 and to the microcontroller 130. An input output/memory control signal generated by the chip select logic 138 is distributed via a line 176 to the SCSI interface circuit 122 and to the data sequencer/DMA controller circuit 126. A read cycle signal generated by the microcontroller 130 is distributed via a line 178 to the firmware ROM 134 and to the external RAM 136. A write cycle signal also generated by the microcontroller 130 is distributed via a line 180 to the SCSI interface circuit 122, the data sequencer/DMA controller circuit 126 and to the external RAM 136. Various other control lines as shown in FIG. 3 extend to provide control signal path between the elements of the control electronics 120.

The host interface circuit 122, which is preferably an enhancement of the features found in the OMTI type 5080 SCSI interface integrated circuit made by Scientific Micro Systems, Inc., of 339 N. Bernardo Avenue, Mountain View, Calif., interfaces the subsystem 10 to the host computing system via a conventional 50 pin SCSI connector. The SCSI interface circuit 122 is con-

figured as a state machine which cycles through its processing states autonomously in accordance with the value set in the loop counter 123 while remaining under the supervisory control of the microcontroller 130.

5 When the microcontroller 130 has provided the SCSI interface circuit 122 with information including the number of blocks to transfer count set into the loop counter 123 and the direction of data block flow, and when the microcontroller 130 has commanded commencement of a block transfer, the SCSI circuit 122 will transfer that number of blocks from the cache buffer 124 as addressed by the DMA controller 126 to or from the SCSI bus in accordance with the SCSI communications handshake protocol with the host computing system.

The SCSI circuit 122 includes an internal buffer for latching and holding SCSI command values received from the host or "initiator" and can assert a BUSY state in accordance with the SCSI protocol. When the microcontroller 130 becomes available for I/O supervision, the SCSI circuit 122 calls for service over the interrupt line 217, and thereupon the microcontroller 130 may direct the SCSI circuit to obtain and forward the SCSI command in order to begin command decoding and processing. In order to obtain such information, an address value from the microcontroller 130 is strobed into the SCSI interface circuit 122 on the falling edge of the address latch enable signal; then, data is strobed from or to the bus 160 by the read or write signals on the lines 178 and 180, providing that the SCSI interface circuit 122 is being addressed by the microcontroller 130.

The microcontroller 130 may also command the SCSI interface circuit 122 to perform direct memory access (DMA) operations between the SCSI bus 170 and the cache memory 124 in either synchronous or asynchronous mode. The interface transfer block loop counter 123 within the SCSI interface circuit 122 may be directly set and incremented by the microcontroller 130 so that block counts may be updated and modified to enable block transfer operations to continue uninterrupted during the microcontroller's second phase or "servo time" when the microcontroller 130 is performing its servo control supervision operations and is therefore unavailable to supervise input/output activity. This feature enhances the rate of overall data throughput.

The SCSI interface circuit 122 reads or writes data from/to the cache buffer 124 over the nine line DMA bus 168 (eight data bits and one parity bit). The transfer 50 is controlled directly by the data sequencer/DMA controller 126 which handles addressing of the cache buffer via the cache buffer address bus 166. When the data sequencer/DMA controller 126 is operating in a page mode, data transfer between the cache buffer 124 and the SCSI interface circuit 122 can occur at up to 6.5 megabytes per second. This high DMA transfer rate enables the SCSI interface circuit 122 to communicate over the SCSI bus at a synchronous data rate of 4.0 megabytes per second, while the data sequencer/DMA controller circuit 126 simultaneously controls disk to cache buffer data transfers and cache buffer RAM refresh operations.

The data sequencer/DMA controller 126 combines in a single integrated circuit chip the structures and functions of the data sequencer circuit 413 and DMA memory controller circuit 417 as described in U.S. Pat. No. 4,639,863, incorporated by reference. In addition, the disk transfer block loop counter 127 within the data

sequencer portion of the circuit 126 may be directly set and incremented by the microcontroller 130, so that transfers of blocks of data between disk data surfaces and the cache buffer 124 may be carried out without interruption as the data sequencer loops through its states in accordance with the loop count held in the counter 127, while the microcontroller 130 is performing its servo control operations.

The data format placed in each data track may be generally in accordance with the 512 user data bytes per sector format as set forth in the present assignee's subsidiary's U.S. patent application Ser. No. 07/098,913 filed on Sept. 21, 1987, now U.S. Pat. No. 4,914,530 incorporated by reference. Logical data block sizes which are integral multiples of the 512 byte sector size are easily provided by concatenating physical sectors together as single logical units. Thus, block sizes of 1024 and 2048 bytes are easily provided within the subsystem 10. A one to one interleave ratio is presently preferred in the actual format of data sectors in each data track.

The read channel integrated circuit 128 is similar to the circuits 409 and 411 of the referenced U.S. Pat. No. 4,639,863. In addition, the circuitry 128 supports two data transfer rates: a first, faster rate for outside region of data tracks, and a second, slower rate for an inside region of data tracks, as more particularly explained in U.S. patent application Ser. No. 07/052,709, filed on May 20, 1987, now U.S. Pat. No. 4,825,321 entitled "modular unitary disk file subsystem having increased data storage capacity", incorporated by reference.

#### Bi-Phase Operation of Microcontroller 130

As was the case of the single microcontroller supervisor of the disk drive subsystems described in U.S. Pat. Nos. 4,639,863 and 4,669,004, incorporated by reference, the microcontroller 130 divides its time between two time divided, repeating phases: a first phase for supervision of data block read/write transfer operations carried out by the SCSI interface circuit 122, cache buffer memory 124, data separator/DMA controller 126 and read channel 128; and, a second phase for servo control of head position of the actuator structure 80 and However, in the subsystem 10, time division between, and overall organization of, these tasks has been tailored in such a manner that performance of the microcontroller 130 has become more optimized. This optimization has further contributed to reduced average access time and enhanced overall data throughput performance of the subsystem 10.

As shown in FIG. 4 when the subsystem 10 is in a track following or "on track" operational mode, a processing cycle of the microcontroller 130 takes about 180 microseconds and is divided between a 75 microsecond servo phase and a 105 microsecond main loop phase. (The main loop is discussed hereinafter in conjunction with FIGS. 9 and 10).

During track seek operations, when track crossing information from the optical encoder assembly 100 is coming in much more rapidly, the bi-phase processing cycle is reduced in overall length to 90 microseconds, in which 60 microseconds are devoted to servo phase processing and 30 seconds are given to main loop phase.

During a track settle operational mode carried out at the completion of track seek but before the actuator assembly is stably following the destination track cylinder location, the overall processing cycle is 120 microseconds long, in which 80 microseconds are for servo processes and 40 microseconds are for main loop tasks.

With this particular time division arrangement tailored to operational tasks, the microcontroller 130 is never off line from the main loop for more than about 90 microseconds. Thus, any SCSI command received from the host computing system, may be recognized by the microcontroller 130 within a 100 microsecond window. Also, if a SCSI initiator device such as the host computer begins arbitration of the SCSI bus while the microcontroller 130 is executing servo time routines and unavailable, the SCSI interface circuit 122 automatically asserts a BUSY. The 100 microsecond window margin is important for smooth throughput of data in accordance with the ANSI standard SCSI communications convention. At the same time, faster track accesses and settles are carried out during servo time, since the microcontroller 130 is given more processing time during these servo-intensive, relatively less frequent, operational modes.

Preferably, the microcontroller is implemented with a 16 bit NEC type UPD 78312 microprocessor. This particular device includes multiplexed analog input and pulse width modulation output ports in addition to the digital data and address buses, control lines, on-board program memory 132 and random access memory 133, shown in FIG. 3.

In the subsystem 10 the on-board program memory 132 and random access memory 133 are used for storing program steps and live time values which are execution time critical, such as servo values. Since these memories are fully integrated with the microcontroller 130, access times to values stored therein are effectively twice as fast as compared to access times using the external program memory 134 and random access memory 136. By judiciously dividing control program subroutines and storage of live time values between the internal memories 132 and 133 and external memories 134 and 136, considerable improvement is realized in processing speed and efficiency of the microcontroller 130 over the referenced prior, single processor designs.

Overall main loop phase program execution followed by the microcontroller 130 is outlined in FIG. 9. Therein, any of the reset signals, such as the power-on-reset signal from the circuit 144 causes the microcontroller 130 to begin executing an initialization process 202. Once that process is completed, the microcontroller 130 enters a main loop 204. The main loop 204 follows a subroutine pointer table arrangement as set forth in FIG. 10. That is to say, during main loop time, the microcontroller 130 follows the path of the main loop 204 in executing routines and subroutines. As such routines are incrementally carried out, increments 206 are recorded in memory. These increments are used to control a subroutine pointer 208 which addresses a subroutine pointer table 210. This table 210 sets forth jump addresses for jumps to subroutines stored either in the on board program memory 132 or external program memory 134.

Three classes of interrupts enter the main loop 204: a servo interrupt 212 which occurs when an internal clock within the microcontroller 130 has determined that servo time has arrived (i.e. completion of an analog to digital conversion scan cycle of P1 and P2 encoder values). When a servo interrupt is received, main loop execution is halted at a particular program increment 206. The subroutine pointer 208 is then set to point to the next sequential step or subroutine in the table 210 to be carried out during the next main loop phase, and then servo service routines 214 are executed during the servo

phase. These servo routines 214 will be explained in greater detail hereinafter.

After completion of the particular servo service routine phase, whether the servo routine be on-track, seek, microstep or settle, a return is made to the main loop 204. At any time during execution of the main loop phase a SCSI command received at the SCSI interface circuit 122 will cause that circuit to send a SCSI interrupt signal 216 via a line 217 to the microcontroller 130. When a SCSI command interrupt 216 is received during a main loop phase, a SCSI command decode routine 218 is entered, and the command is therein decoded.

Once a particular command is decoded, an appropriate service routine is pointed to and execution of the routine begins. There are virtually an unlimited number of commands that may be decoded and carried out. Several of the most frequently executed commands are given in FIG. 9. These commands include FORMAT 220, STATUS 222, WRITE 224, READ 226 (the other commands supported being lumped in the block 228). Execution of each SCSI command may require use of the same subroutines. For example, the WRITE and READ commands 224 and 226 each require the microcontroller to seek (or microstep) and settle at a particular track location where data blocks are to be written or read. As part of these commands, seek and settle subroutines are executed.

Once a SCSI command has been completed, a command completion processes block 230 is entered, and housekeeping appropriate to complete the particular command execution process is carried out, i.e. values are saved, counters and memory locations are cleared, etc. At the end of the completion processes block, control program execution returns to the main loop 204.

Other interrupts, such as a motor speed interrupt, enter the main loop 204 at a block 232. The spindle motor controller circuit 142 includes a tachometer circuit which monitors disk angular velocity and signals the processor 130 if the spindle motor 52 and disks 64, 66 and 68 are not up to speed. In this event, the microcontroller 130 generates an appropriate status byte and sends it through the SCSI interface circuit 122 to the host computing equipment.

#### Servo Architecture

The servo architecture of the subsystem 10 employs both velocity and position servo loops, velocity mode for track seeking operations and position mode for settling, microstepping (short seeks) and for on-track centerline following operations.

#### Servo Fast Seek Mode FIG. 5

A model of the velocity information based servo architecture of the microcontroller 130 as configured during track seek operations is depicted in FIG. 5. This servo mode is employed with all seek operations in which the destination cylinder location is in excess of 24 cylinders away from the departure cylinder location. In this mode, the servo service routine interrupt occurs every 90 microseconds.

When current is applied to the rotor coil 82, the actuator structure 80 moves radially inward or radially outward, depending upon the polarity of the driving current. As the actuator structure 80 moves one way or the other, the microlines of the glass scale 90 interrupt the light paths of the encoder 100 and result in the two sinusoidal-like analog phase signals P1 and P2, with the signal P1 leading or lagging the P2 signal by 90 degrees,

depending upon the direction of movement. When the analog P1 and P2 signals are applied to the comparator 148, two digital signals DIG P1 and DIG P2 result. The period of each signal DIG P1 and DIG P2 marks two cylinder boundaries.

These digital signals DIG 1 and DIG 2 are respectively applied to decrement two track downcounters 328 and 330 within the microcontroller 130 which have been preloaded with a value corresponding to one half of the number of cylinders to seek during the particular seeking operation. This number is based on the fact that the actuator structure 80 has previously been calibrated, and that the position of each data head is known with respect to a departure cylinder location, since the track ID corresponding to that location has been read and provided via the data sequencer/DMA controller circuit 126. Thus, if the departure cylinder location is 622 and the seek is to be radially outward to track 400, for example, a value of 111 (half of the total seek of 222 tracks) is loaded into each track counter. Once actuator motion begins in the proper direction, the down counters 328 and 330 will decrement on rising and falling edges of the DIG 1 and DIG 2 signals.

A 1.5 megahertz clock 321 provides a sampling rate to a free running counter 322. Two 16 bit clocked latches 324 and 326 capture the real time count of the free running counter at a predetermined sampling rate. On a first track crossing clock edge a count reached by the free running counter 322 is latched in the latch 324. On the next occurring edge, the count reached by the free running counter 322 is latched in the latch 326. The counts are differenced by a TACH summing junction 332. The difference between the values held in the latches 324 and 326 is a measure of the time elapsed between the last two track crossings and provides a real time velocity feedback signal VEL.

At the same time, outputs from the track counters 328 and 330 are combined in a tracks-to-go summing junction 334 to provide a total of the tracks remaining to be crossed and the resultant value is applied to address an appropriate trajectory value stored in a trajectory profile look-up table 336 in the external read only memory 134. A ratio value, VELNORM, of actual velocity VEL to reference velocity VELREF is calculated in a VELCALC junction 338 in order to normalize the difference between actual velocity VEL and reference velocity VELREF irrespective of magnitude thereof. In calculating the normalized error signal VELNORM (which is performed to reduce bandwidth of, and thereby stabilize the seek loop based on velocity information) the velocity reference VELREF is multiplied by 128 and then divided by real time velocity VEL. If actual velocity corresponds to profile velocity, then the VELNORM value put out from the junction VELCALC is 128. In any event, VELNORM lies in a range between zero and 256.

A feed forward current value FC is calculated by the microcontroller 130 at a process 340 to provide a base current value, depending upon the nature of the seek. The feed forward value FC is an a priori prediction of current expected to be required to carry out the seek. It is based on information which quantify the operating characteristics, some of which are developed during initialization calibration routines, discussed hereinafter. The feed forward value FC allows more accurate adherence to the desired seek trajectory for a given velocity servo loop bandwidth.

Basically, a nominal current waveform is preestablished for each seek length. The feed forward waveform value FC corresponds to the actuator current needed to keep the actuator on the idealized trajectory. The normalized, signed velocity signal VELNORM is added to the feed forward value FC to correct for any deviations from the reference trajectory due to friction, torque constant variation, etc. An example of a feed forward waveform value FC is set forth as FIG. 6A and illustrates an initial positive full current increment for causing maximum acceleration, a zero current increment for a coast interval and then a negative 80 % current increment for deceleration. Resultant velocity is graphed as FIG. 6B.

For example, in the 222 track seek example set forth above, the feed forward current value FC may be current full on in order to command maximum torque until either e.g. 43 inches per second of limit velocity (FIG. 6B) is reached at which point a zero current value coast increment is followed or the decelerate switch point, e.g. 111 tracks or some lesser or greater number is reached, depending upon the initialization information. During coasting mode, a substantially constant velocity of e.g. 43 inches per second is maintained. The switch point detection process compensates for the inductance of the actuator by switching to deceleration current mode approximately one millisecond in advance of convergence of measured velocity VEL and the switchpoint of the reference velocity trajectory FC. This look-ahead approach minimizes overshoot of the actuator trajectory. The switch point velocity is recalculated from the command velocity FC for each servo phase in the accelerate mode.

Continuing with the example of a 222 track seek (FIG. 6A), after the first 111 tracks have been crossed, the feed forward current waveform value FC may switch to a reverse current which is e.g. 80 percent of the full current, and this reverse current is applied until the actuator reaches the vicinity of the destination track and its velocity has slowed to almost zero (FIG. 6B). During accelerate, coast and decelerate modes the velocity servo loop is closed and feedback corrects the trajectory.

The normalized error signal VELNORM is added to the a priori feed forward value FC at a process 342 which yields an actuator coil current value I which is pulse width modulated by a pulse width modulator 312 within the microcontroller 130. The pulse width modulated I value is converted into an analog driving signal in the filter and PWM to analog converter 141. The pulse width modulator repetition frequency is 23.8 KHz and the filter 141 functions as a 3rd order Chebyshev filter for minimal passband phase loss (4.5 degrees) with a cutoff of 8 KHz.

The converted analog driving value is then amplified into a suitably signed driving current in the rotor power amplifier driver circuit 140 which preferably includes SGS L2722 dual power operational amplifiers to deliver up to one-half Ampere maximum current. Separately controllable gain modes for the operational amplifiers are provided for track seeking and track following operations. High gain is commanded during track seeking operations. Snubber networks are provided to eliminate high frequency switching spikes.

The driving current put out by the driver circuit 140 is then applied to the rotor coil 82 in order to control its torque in order to cause the actuator structure 80 to

approach and remain in correlation with the reference trajectory throughout the seek operation.

#### Servo Angle Seek Mode, FIG. 14

5 A settle servo loop employing an arctangent look up table approach is described in commonly assigned Assignee' U.S. Pat. No. 4,516,177, particularly in conjunction with FIG. 7 thereof, the disclosure of which is hereby incorporated by reference.

10 In the disk drive of the present invention, while the angle seek mode is a velocity servo used for controlling short seeks and for controlling arrival and settle portions of long seeks, it has aspects of the architecture of the track following servo, FIG. 7 herein. (With one

15 track resolution the fast seek mode position feedback is too coarse be used for the arrival and settling portion of a seek.) Also, there is excessive time delay in the velocity feedback servo loop fast seek mode at low angular velocities of the actuator structure 80. In this mode the 20 microprocessor servo service routine interrupt occurs every 120 microseconds. A model of the servo angle seek mode is graphed by the block diagram of FIG. 14.

25 The angle seek mode divides each cylinder into 128 angular increments in order to overcome these problems at the lower angular velocities. With a track density of 1000 tracks per inch, positioning resolution is 7.8125 microinches per degree of encoder phase rotation, there being 360 degrees provided for four adjacent cylinders.

30 At about four cylinders short of the destination cylinder location, the velocity information servo depicted in FIG. 5 begins sensing angular position information in the fashion provided by the track following position information servo structure depicted in FIG. 7; and, it operates in an angle seek mode in which angular information samples are provided at a higher rate than during normal track following operations.

35 The analog outputs P1 and P2 of the optical encoder assembly 100 are received at two multiplexed channels 40 of the analog to digital converter of the microcontroller 130. These signals are used to compute a corresponding angle in a range between zero and 511, indicating a position on an x-y lissajous circle, FIG. 8. The analog to digital process has a conversion time of 30 microseconds per channel. In the angle seek mode the P1 and P2 values are scanned and converted to digital values by internal firmware programming of the microcontroller 130. Once the two digital values are ready, the angle seek interrupt service routine is entered. The first step is 45 to compute the measured angle for this interrupt. This angle is differenced with the angle from a previous sample. This difference results in a signed number of degrees travelled between interrupts, i.e. an ANGLE VELOCITY value.

50 55 The ANGLE VELOCITY or signed number of degrees per interrupt is summed in a 16 bit position error register to provide an ANGLE ERROR value. The ANGLE ERROR value indicates the number of degrees to go to the desired target angle on the four cylinder lissajous circle, FIG. 8. The signed 16 bit ANGLE ERROR value is sufficiently large to accomodate up to plus or minus 255 cylinder locations.

56 The ANGLE VELOCITY value is multiplied by a gain factor (Ktach=6). The product is used as the velocity feedback value Vel to be compared with a commanded value Fc. The ANGLE ERROR value is multiplied by a gain factor (Kpos =  $\frac{1}{2}$ ) in order to generate a position dependent command velocity Fc. The maxi-

mum command velocity in the angle seek mode is limited to plus or minus e.g. six inches per second. The command velocity profile  $F_c$  is linear with degrees to go. As the angle error nears zero, the command velocity  $F_c$  becomes zero. The difference between the command and measured velocity is multiplied by a gain factor  $K_{fs}$ . The error is added to a seek no torque value SEEK NULLI and put out to the pulse width modulator of the microcontroller 130 and thence through the converter/filter 141 and amplifier 140 to the coil 82 of the actuator. Upon transition from the fast seek mode to the angle seek mode, a calculation is performed within the microcontroller 130 to load the ANGLE ERROR register with the correct number of degrees to yield an ANGLE ERROR zero value at the final target angle (destination cylinder location).

Thus, in the angle seek mode the actuator structure 80 is commanded to move linearly to the destination track location by feeding precise angle reference values into the FIG. 7 servo loop until the final destination angle (position within the destination track corresponding to predicted centerline thereof) is reached. The advantage of this particular implementation of fine or angle seek mode is that it provides wide bandwidth with adequate phase margin for good settling characteristics.

With reference to the FIG. 14 functional model, within the microprocessor 130, a position reference block 300 supplies a digital reference angle value to a summing junction 302 in which the one half gain weighted actual angular position is subtracted. The difference comprises the ANGLE ERROR value which is multiplied by a gain factor of one half at a block 304. Weighted velocity (having a gain factor of six times) is subtracted from weighted ANGLE ERROR at a summing junction 306 to produce the position dependent command velocity  $F_c$ , and this value is weighted by a factor of 1.3 in a block 308 and then sampled and held digitally in a register 310 and is then put out from the microprocessor 130 via a pulse width modulator 312 to the filter 141 having a predetermined transfer function  $F(s)$ . The filter 141 is a third transfer function having a cutoff at approximately 7 KHz. The filtered command velocity signal  $F_c$  is then amplified by the amplifier 140 and sent to the actuator 82 which is modelled as a double integrator. A first differentiator 314 (implicitly including the optical encoder structure 100) yields a velocity feedback signal which is six times weighted at a block 316, and a second differentiator 318 (also implicitly including the optical encoder structure 100) provides a position feedback signal which is one half times gain weighted at a block 320.

#### Settle Mode

At about five degrees from the predicted destination angle, a settle mode is entered. In this mode, the microprocessor servo service routine interrupt occurs every 120 microseconds. The servo bandwidth is 300 Hz and has 40 degrees phase margin. Lead/lag compensation is included in the servo loop. In the settle mode servo loop an integrator is also implemented within the microcontroller 130 in order to eliminate any DC error, such as that due to friction in the actuator spindle. At this point the integrator starts adjusting the NULLI values so as to drive the DC error to zero.

The settle mode difference equation is: Not self settled (integrator disabled):

$U_k = 12 * [X_k - .915(X_{k-1})] + \text{NULLI}(0)$   
Once self settled (integrator enabled):

$$\text{NULLI} = \text{NULLI}(0) + \frac{\Sigma^k X_k}{60}$$

where:

$U_k$  = Settle mode output,

$X_k$  = ANGLE ERROR,

$X_{k-1}$  = Previous ANGLE ERROR, and

NULLI(0) = Predicted NULLI.

Once actual position is within e.g. plus or minus three degrees of nominal angular position for e.g. seven successive P1/P2 servo samples, the actuator is deemed to be settled and the servo mode switches to the on-track position. information servo structure depicted in FIG. 7.

#### Servo Track Following Mode, FIG. 7

A model of the position information based servo architecture of the microcontroller 130 configured during track following operations is depicted in FIG. 7. The microcontroller service bi-phase duration in this mode is 180 microseconds, as shown in FIG. 4. The servo interrupt service routines require about 75 microseconds, thereby enabling the SCSI main loop firmware to execute its routines during the remaining 105 microseconds. The servo track following service routines implement a lead filter and an on-track integrator as in the angle seek servo configuration.

The difference equation for the FIG. 7 servo track following mode is:

$$U_k = X_k + 8 * (X_k - (X_{k-1})) + \frac{\Sigma^k X_k}{80}$$

The analog P1 and P2 phase signals from the optical encoder circuit 100 are converted into digital values by an analog to digital conversion process 344 carried out within the microcontroller 130. The analog values are converted into a  $\sin x - \cos y$  angle value by an arctangent table look-up which is similar to the process described in the present assignee's U.S. Pat. No. 4,419,701, incorporated by reference. This angle value is analogous to the four cylinder circle lissajous figure, as depicted in FIG. 8 in which the digitized four phases P1, P2, BAR P1 and BAR P2 define over the locus of the lissajous circle four cylinder locations in 512 digital angle increments. It is important for positional accuracy that the DC offset position of the FIG. 8 lissajous figure be maintained during operation of the subsystem 10.

The digital angle values 0-511 of the FIG. 8 circle represent four cylinder locations centered at digital values 0 (512) (track 0), 384 (track 1), 256 (track 2) and 128 (track 3, etc.). Thus, there are 128 digital increments or steps throughout each data cylinder location. Track 0 (and track 4, 8, 12, 16, etc.) is bounded, for example between digital angle values 63 and 447, while track 1 (and track 5, 9, 13, 17, etc.) is bounded between digital angle values 447 and 319, etc. The digital angle values wrap around the value 511 to zero.

The actual angle  $A_{act}$  measured by the optical position encoder structure 100 is differenced with a reference angle  $A_{ref}$  in a summing junction ASUM 346 which results in a servo correction angle ANGLE ERROR. The reference angle ANGLE ERROR is derived by the microcontroller 130 for a particular track loca-

tion from centerline offset and offset slope information obtained during the optical encoder servo calibration routines carried out during initialization and intermittently during operation of the subsystem 10. The correction angle ANGLE ERROR is then further modified by a phase lead-lag process 348 conventionally provided for servo loop stability and is then pulse width modulated and put out as a track follow mode actuator coil current Ifollow by the pulse width modulator 312 of the microcontroller 130.

During a seek operation just preceding the track following operation, the reference data for the particular head and phase (whether optical phase 1, 2, 3, or 4) of the destination track is read from the external RAM 136 into the internal RAM 133 in a block move.

The current Ifollow is then filtered and converted into an analog value by the filter/converter 141 and then amplified by the actuator power amplifier 140. It is then applied to the actuator coil 82 to generate whatever torque is required to cause the actuator structure to move to the angular position commanded by the microcontroller 130.

As already explained in the discussion of angle seek mode above, microstepping from track to track during settling, and seeks of e.g. twenty four tracks or less, is accomplished by adding or subtracting digital new angle values into the summing node ASUM from the angle reference source in order to cause the actuator to move to the new angular position. During settling at the end of a seek operation and during microstepping, position samples are obtained and processed from the optical encoder 100 more frequently than when the actuator structure is following a particular track location in the following mode. This increased sampling rate increases the servo phase margin and decreases settling time, thereby improving average seek time performance of the subsystem 10.

A bump detect feature of the track following servo prevents writing of data in the event of an external shock. A flag is set when the drive is writing data that enables bump detection via the servo interrupt. A bump is detected by testing the current value of ANGLE ERROR. If the off track error exceeds plus or minus .90 microinches, for example, the write function is aborted by writing to a register in the data sequencer 126. The servo service routine then sets a flag that indicates to the WRITE firmware that a bump has occurred. The WRITE command execution code will then retry to write the data block stream, beginning at the sector where the bump was detected.

A "write unsafe" service routine monitors the output of a signal from the read/write preamplifier 96. In the event that conditions such as a loss of write current, or no data pulses, are detected during WRITE command execution, the write unsafe service routine aborts the write operation and sets a flag indicating unsafe write condition to be read by the WRITE service routines.

A "seek back" feature of the track following servo mode is invoked in the event that ANGLE ERROR exceeds plus or minus one and a half tracks. This may occur if a very large shock force were applied to the drive. If this happens, a flag called OFF TRACK is set, and the subsystem 10 thereupon cannot perform a new seek until this flag is cleared. In seek back, the servo switches back to angle servo mode which has the full torque capability of the actuator 80 available for making the positional correction. The seek back mode will drive the actuator structure back to the correct servo

reference angle, even if the shock force has driven the actuator several cylinders off track. The angle seek mode then initiates the settle mode to reset and test at the correct angle. Then the track following servo mode is restarted and the OFF TRACK flag is cleared. The subsystem 10 has recovered from the shock.

#### Initialization Process 202

When power is first applied to the subsystem 10 the microcontroller 130, SCSI interface circuit 122, and data sequencer/DMA controller 126 are first initialized. If an autostart jumper is installed, nothing further happens until a START command is received across the SCSI interface. If the jumper is not installed, or if a START command is received with the jumper in place, the spindle motor 52 is started and default servo and head gain values are loaded into appropriate locations of random access memory. Inward torque is then applied to the actuator structure 80 to move the heads 94 to the inner landing zone LZ in order to make sure that the actuator is at a known position.

The cache buffer 124 is loaded with "ones" (hexadecimal FF bytes) and then checked. The cache 124 is then loaded with "zeros" (hexadecimal 00 bytes) and again checked.

Spindle motor speed is then monitored until it is within one percent of 3662 RPM. The analog P1 and P2 values put out by the optical encoder 100 directly to an A/D port of the microcontroller 130 are then checked to be sure that they lie within a reasonable range. The digital P1 and P2 values put out by the comparators 148 are also checked and verified at the microcontroller 130.

The actuator 80 is then commanded to move to a midstroke position. In this subroutine the NULLI variables are set to default values. (NULLI is a current value which results in current in the actuator coil 82 which produces a torque equal to, and in a direction opposite from, any torque on the actuator 80 that would change its position, such as a bias spring force attributable to the flexible printed circuit, deflection from airflow generated by disk rotation, meaning that actuator actual position correlates to commanded position without positional error). The current cylinder register is set to 400 and the target cylinder is set to zero, which thereupon causes an outward 400 cylinder seek from the landing zone LZ and places the heads 94 at a midrange of the data surfaces.

Encoder center values are computed for both of the analog P1 and P2 values then being received by the microcontroller 130. An attempt is then made to read the format of the nearest track being followed by head zero to determine the actual track number recorded in the format.

If a track ID was successfully read, the initialization process 202 proceeds directly to an optical encoder servo calibration procedure. If not, the actuator 80 is commanded to microstep outwardly via the angle seek mode, e.g. 48 tracks at a time, until an outer crash stop is reached. Once the outer crash stop is reached, the actuator 80 is commanded to microstep inwardly while the microcontroller monitors the read channel via the peak detector amplifier 146, looking for the servo bursts written in the four outermost tracks. If the servo bursts are located, the microcontroller 130 has established a reference location for the heads and prediction servo initialization begins at track -4. If not, then a NO SERVOs routine is entered which places the actuator at

cylinder zero, defined as the 18th track located inwardly from the outer crash stop.

Subsystem data, such as initial configuration values, a track defect map, a drive serial number, etc., is now read from a protected location, such as cylinder -3. This location is not directly accessible to the host computing system. Whatever configuration is specified by the information so read is then carried out within the subsystem 10. Typically, this information provides the firmware with values indicating whether an 80 megabyte drive with six heads is present, or whether a drive having greater or lesser heads/disks is present, etc.

A head A/B burst to encoder microstep calibration factor ( $K_{ab}$ ) is obtained and stored during initialization for each data transducer head 94. This factor is related to the particular width and gain characteristic of the head itself as determined by head manufacturing tolerances. This information enables the microcontroller 130 to know for each head how many degrees of compensation are required in order to move the particular head a known distance so as to be able to reach exact centerline alignment with the track to be followed. This calibration is only carried out in the initialization routine, as head width does not change significantly with temperature variations.

In normal operation a formula is used to compute the number of encoder degrees to change in order to set the angle reference to correspond with track center:

$$E = \frac{A * K_{ab}}{[(A + B)/2]} - K_{ab}$$

where:

$E$ =encoder correction (in degrees),

$A$ =A burst reading (0 to 255),

$B$ =B burst reading (0 to 255), and

$K_{ab}$ =calibration factor.

For odd cylinder locations,  $A$  is replaced with  $B$  in the numerator of the above equation. The  $[(A + B)/2]$  factor is the average of the  $A$  and  $B$  servo digitized amplitudes and normalizes the calculation for amplitude. As mentioned above, a nominal default value is used during power on initialization. Then, the head calibration factor  $K_{ab}$  is accurately derived and stored for each head, as follows:

1. Seek to an even cylinder location.
2. Equalize A/B servo amplitude values using the default  $K_{ab}$  calibration factor within  $+/-$  one microstep.
3. Step off a known number of microsteps toward the outside diameter (e.g. 16 microsteps).
4. Solve the above equation for  $K_{ab}$  with all other variables known:

$$K_{ab} = \frac{E}{\frac{A}{[(A + B)/2]} - 1}$$

Servo calibration of the optical encoder 100 begins with the heads positioned at cylinder -8 and head 94(0) (track -8). The servo index interrupt 212 is enabled, which means that the index marker signal 173 on the line 174 causes the microcontroller jump to a routine to acquire and digitize peak amplitude values of the A/B servo bursts recorded on surface 0 immediately following the index marker signal. A timer is also started with occurrence of the index marker signal. The difference in peak values is determined and the track center encoder angle (OD) is computed and stored for head 0. Then,

head 94(1) is selected and 2.8 milliseconds later the A/B servo bursts are read for head 94(1) and the difference in burst amplitudes is determined and the encoder angle (OD) is recorded for head 1. This process is repeated 5, 6, 8, 4, and 11.2 milliseconds after index for each of the other heads 94(2), 94(3), 94(4) and 94(5) for cylinder -8. Then, this process is repeated for cylinders -7, -6 and -5, so that angle (OD) values for the four tracks corresponding to each of the four phases defined by the optical encoder 100 are separately sensed and recorded. The outer diameter servo cylinders and surfaces have now been read and angle (OD) angle error values recorded in memory.

The same process is now carried out for the inside diameter servo cylinders and heads. The actuator 80 is commanded to seek to track 838, and the above-described process of obtaining and recording error values for the heads at cylinders 838, 837, 836 and 835 is carried out. Then, for each head and track phase, a slope value, comprising the difference in angle for each head at track phase P1, P2, BAR P1 and BAR P2, is calculated and recorded by correlating the angle errors from cylinder -8 with cylinder 835, cylinder -7 with cylinder 836, cylinder -6 with cylinder 837 and cylinder -5 with cylinder 838. These slope values, called ANGLE SLOPE, are then recorded in memory.

AGC gain is also determined during initialization, and also during calibration updates to control the AGC gain factor of the read channel circuit 128 as controlled by the pulse width modulator output through the filter 150. Since this variable is provided to compensate for gain variations due to head to disk velocity reductions as the actuator moves from outer cylinders to inner cylinders and due to thermal gain drift of the read/write head preamplifier electronics 96, the A/B gains of all of the heads 94 are averaged for an outer and an inner cylinder location and an overall AGC reference value and an overall AGC slope value is determined and recorded. Thereafter, when a seek is made, an AGC value for a particular track location is calculated and applied as an AGC value.

The NULLI or on-track current required to keep the head structure in track-following alignment will have a different value when the cylinder location is approached from different seek directions. Thus, during initialization, a hysteresis calibration is carried out by deriving and storing a value for seek in the inward direction and a value for seek in the outward direction. The hysteresis calibration is used to predict the required on-track NULLI current for a given track and seek direction. This value reduces settling time by priming the integrator established during the settle mode with a null torque value that is closer to final value than otherwise.

When all of the initial tasks required to set up the subsystem 10 for data read/write operation have been completed, the drive ready flag is then set, and initialization is complete.

#### Main Loop 204

The main loop process 204 checks to see if an ID switch flag is set. If so, the subsystem ID number available at the SCSI interface circuit 122 to the host computing system is changed. If any SCSI reconnects are owed, reselection arbitration is started for the initiator host system. If the drive has been reserved by a particular initiator, this fact is determined. If any initiator is

queued on a reserve list, reselection arbitration is started for that particular initiator. If a self seek jumper is installed on the circuit board 58, a self seek service routine is called.

If a pre-fetch operation is active, meaning that the subsystem 10 either is transferring subsequent data blocks or about to transfer subsequent data blocks from the disk to the cache buffer 124 in anticipation that such blocks will be requested by the host, based on the most recent block requested, then the main loop branches to a series of pre-fetch service routines which are carried out until completed.

If a pre-fetch operation is not active or is incomplete, then the main loop process calls the next background subroutine pointed to in the subroutine pointer table 210. One such subroutine is the check thermistor subroutine. In this routine the temperature sensed by the thermistor 105 is read and converted to a digital value and added to a running sum. After 90 such readings, the running sum is divided by 90 to obtain an average temperature. This average temperature is then compared to a thermistor base value in order to determine whether the average temperature has increased or decreased more than a predetermined threshold amount from the base value.

If sensed average temperature has risen above or has fallen below a threshold amount, such as 2 degrees Centigrade from the last reading, servo prediction recalibrate subroutines are called. During a prediction update, the microprocessor 130 will position the actuator over the outside diameter (OD) servo cylinders and read the A and B burst amplitudes for each head and optical encoder phase (See FIG. 12). The computed new angle references are stored in a table. The actuator is then positioned over the inside diameter (ID) servo cylinders and the A and B burst amplitudes for each head and optical encoder phase are read. The encoder reference angle measured on the inside diameter is differenced with that of the same head and phase on the outside diameter. A slope is then computed and stored, enabling the seek servo routine to linearly interpolate the prediction angle for a head as a function of the requested destination or seek target data cylinder location. Typically, the prediction angle for a given head and phase will vary over temperature as shown in FIG. 13.

During servo prediction recalibration, the X-Y center of the optical encoder P1 and P2 values is recalculated and compensation values are stored in order to eliminate any DC offsets due to encoder thermal drift. Values enabling determination of the NULLI or on-track current vs. track position and seek direction are also obtained and stored in memory during calibration.

During the servo prediction recalibration routines, the head gain correction factors Kab for each head determined during initialization are used. A timer is established within the microprocessor 130 and monitored as well as the thermistor 105, so that in any event, the servo prediction recalibration process is repeated periodically during continuous operation of the subsystem 10, e.g. once each hour.

When a background subroutine is completed, the subroutine pointer 208 is incremented, and then the next background subroutine in order in the table 210 is called and executed. In this way, a wide variety of background subroutines may be carried out progressively in an orderly fashion, and, new subroutines may be conveniently added as may be required for a particular disk

subsystem configuration merely by adding jump addresses to the subroutine pointer table 210 and adding the subroutines to available space in the firmware memory 134.

The main loop then tests whether a SCSI command has been received at the SCSI interface 122. If not, the main loop returns to test for prefetch activity. If a SCSI command has been received, the prefetch is aborted after a minimum prefetch operation has been completed. The main loop process is then left, the SCSI command is decoded and then processed. After the command is completed, a return is made to the main loop; and, execution processing of a particular background subroutine in the table 210 is resumed in accordance with the location pointed to by the subroutine vector pointer 208. Thus, subsystem delays during command execution will be limited to those of seeking to and finding the correct sector on the disk surface.

#### SCSI Command Decode 218

The host computing environment, denominated an initiator, may send a wide variety of commands to the subsystem 10 including the Format command 220, Status command 222, Write command 224, Read command 226 and other commands 228 such as Test Unit Ready, Rezero Unit, Request Sense, Reassign Block, Seek, Inquiry, Mode Select, Reserve, Release, Copy, Mode Sense, Start/Stop Unit, Send Diagnostic, Read Capacity, Read Extended, Seek Extended, Verify, Read Defect Data, Write Cache Buffer, Read Cache Buffer, for example. These commands are received and stored as byte values in the SCSI interface circuit 122. Once received, the SCSI interface circuit 122 generates a SCSI interrupt 216 and sends it via the line 217 to the microcontroller 130. The microcontroller 130 senses this signal at the step 218, obtains the command from the SCSI interface circuit 122 via the bus 160 and calls a set of routines to accomplish the particular command. The write and read service routines are similar in architecture and will be described in conjunction with FIG. 11.

#### Write/Read Command Processes, FIG. 11

The main processes carried out by a disk drive are read and write. These are very similar processes with a few exceptions. During write, it is very important to determine whether the drive has been bumped or jarred. Thus, the optical encoder phases P1 and P2 are carefully monitored in a bump detect routine in order to determine whether there has been any unexpected change in value. If so, then the write process is immediately discontinued. During read, checking is carried out to determine the validity of the data read from the disk and to correct for any correctable errors, should that be required. The following discussion is related to the read command execution process as exemplary of these two main processes.

When, for example, a SCSI read command is first decoded, the microcontroller 130 sets up the read process 226 by first determining if the number of blocks to read is greater than zero. If not, the process returns to the main loop. If so, values are set for the data sequencer/DMA controller 126 including target final head, target final cylinder and first sector identification. The block size, including ECC bytes is set into the data sequencer/DMA controller 126 and into the SCSI interface circuit 122. A check is made to be sure that the first sector is a legal value.

The cache buffer 124 is scanned to see if the requested data block is already in the buffer because of prefetch activity. If so, then there is no need to reread the data, and the DMA process will be able to transfer the block to the host without further data sequencer activity.

The seek process is then started and head position supervised during seek servo time. A routine is called to calculate the last or highest required address for the cache buffer. The cache buffer memory 124 is arranged as a logical ring, and buffer pointers which point to the next available space in the buffer 124 are set for starting and ending address values; the pointers may have to be rolled over through an address boundary.

A prefetch is calculated which is based upon an assumption that additional blocks in order will be sought by the host, and that throughput is increased if those blocks are read into the cache buffer just after the block being sought is read off the data surface. A main command execution loop, depicted in FIG. 11, is then entered.

Within the write command control process 224 and the read command control process 226 there are three independent and asynchronous activities: a seek activity 232 which is cognizant of movement of the rotary actuator 80 from one track location to another; a data sequencer activity 234 which is concerned with the task of locating data blocks (sectors) at a particular track sector location and moving such sectors to the cache buffer 124 during the read command control process 226, and with locating sector locations and moving blocks of data from the cache buffer 124 into disk track sectors during the write command control process 224; and, I/O (DMA) transfer activity 236 which is concerned with direct transfer of data blocks between the host computer and the cache buffer 124 via the SCSI interface bus 170. While the DMA transfer activity 236 may occur simultaneously with both the seek activity 232 and with the data sequencer activity 234, the latter two activities are mutually exclusive: data cannot be written to or read from a disk surface while the actuator structure 80 is seeking from one track location to another.

When the read or write command process is entered from the command decode 218 in the main loop 204, e.g. the seek process 232 is tested by determining whether seek is active at a logical node 238. If so, a seek active routine 240 is executed which basically tests to see if the seek process has timed out. The seek process 232 may be in a transitional state from active to non-active; and if so, a transition routine 242 is executed. If the seek process 232 is not active, the a seek non-active routine 244 is executed; and if the process 232 is in a transitional state from non-active to active, a second transition routine 246 is executed.

When the data sequencing process 234 is reached, a test is made to determine if the data sequencer 126 is active at a logical node 247. Since the data sequencing process 234 cannot be active during a seek, it executes a sequencer not active routine 248 which tests to see if the seek complete flag has been set. If not, then the data sequencing process 234 proceeds to the DMA process 236.

If the seek complete flag has been set, a transitional state 250 is entered. It tests whether the final head is the target head and final cylinder location is the target cylinder location. It then determines how many sectors are to be read in carrying out this particular read command from the host. A sequencer loop count in the

sequencer loop counter 127 is set equal to the number of sectors to be read.

The identification of the first sector to be read is sent to the data sequencer 126; and, address pointers are set in the data sequencer/DMA controller circuit 126 for the cache buffer memory 124. A timer is set to enforce a sequencer timeout in the event of a failure to locate the first sector location. And, finally, in this transitional state 250 a flag is set to change the data sequencing state 10 from non-active to active. Then, the DMA process 236 is entered.

If the sequencer is active, then a routine 252 is executed. This routine 252 tests whether the data sequencer 126 has completed its tasks. If so, the sequencer active flag is cleared and a transitional routine 254 is executed which tests for possible DMA overrun errors by testing whether the final loop count is other than zero. Since there may be additional sectors left to be read in this particular track, called "possible hot sectors" those 15 sectors are loaded into the cache buffer 124 in anticipation that they may be called for by the host. The data sequencer 126 is tested for any possible errors, and if none, the sequencer active flag is cleared and the DMA process 236 is called.

If the data sequencer 126 has not completed its tasks, a check is made in the routine 252 to determine if the sequencer timer has timed out, indicating difficulty reading the desired data. Then, a check is made to see if there are more sectors to read and whether there is 20 available room in the cache buffer 124 to hold them. If so, the SCSI command interrupt is turned off and a test is made to see whether the data sequencer loop counter 127 may be modified so that additional sectors may be processed while the microcontroller 130 is in servo time. If so, then the loop counter 127 is incremented by an additional count corresponding to the additional blocks requested via the SCSI interface circuit 122. When the sequencer timer times out, the SCSI command interrupt is reenabled and a sequencer done routine is called which sets the sequencer active flag to 25 non-active.

During read mode the data sequencer active state 252, and the transitional state 254 also perform certain error correction code detection and correction processes which are lumped as a block 255 below the DMA I/O block transfer process 236. The data sequencer checks ECC syndrome bytes of each data block read from the disk surface and calls an error correction routine in the event that an error is detected. An error correction process of this type is explained in greater detail in the assignee's U.S. Pat. No. 4,730,321.

The third major logical node in the write/read process is the test as to whether DMA is active 256. If DMA is not presently active, the process follows a non-active routine 258 which may include a transition routine 260 to active.

In the I/O non-active routine 258, a test is made to determine whether the subsystem 10 is disconnected from the SCSI host bus. If the subsystem 10 is connected to the SCSI host, the routine tests whether the number of hot sectors already in the cache buffer 124 is greater than or equal to the total number of blocks required by the host. If not, then a test is made whether the sectors left to read value is less than or equal to the number of sectors to prefetch. If not, then a return is made to check the seek node 232.

If either of these last two DMA node tests is true, then a host reconnect interrupt routine is called and the

SCSI interface circuit 122 is enabled and its data flow direction is set. A check is then made to see if there are any complete blocks present in the buffer 124 ready to be transferred to the host. If so, then a command is executed to be sure that the SCSI interface circuit loop counter 123 is loaded with a count corresponding to the number of blocks in the buffer 124 to be transferred via the SCSI bus 170 out to the host. If it is correctly loaded, then the SCSI interface circuit 122 is reset and commanded to send out the blocks presently held in the buffer by causing the DMA controller 126 to address each of those blocks in turn in the buffer 124 via the buffer address bus 166. The data blocks are read out of the buffer 124 via the buffer data bus 168.

As blocks are sent out to the host, a hot sectors register 262 is decremented by the number of blocks to be read out via the interface 170 to the host. A DMA active bit is then set, and a return is made to the seek active node.

If the DMA is active as tested at the node 256, a DMA active routine 264 is executed. A transition routine 266 from DMA active to DMA not active may also be executed if the end of the DMA block transfer has been reached.

The DMA active routine 264 tests for a verify command which if true clears a bit flag value for host DMA active and then calculates a sectors allocated value stored in a register 268 in main random access memory.

Certain checks are made at the block 255 to see whether there are any parity errors in the cache buffer 124, whether there are any communications errors across the SCSI interface and whether there are any errors associated with the FIFO buffer located in the SCSI interface circuit 122. If there are no errors and if the number of blocks to transfer has now reached zero, a return is made to the main loop 204.

If the verify command is not true, then the DMA active routine determines the number of blocks transferred from the number of blocks to transfer less the count held in the SCSI interface block counter 123. If the number of blocks transferred is greater than zero, then the sectors allocated register 268 is set equal to the number of blocks transferred times the sectors per block. The blocks to transfer value is set equal to the total number of blocks less the number of blocks transferred. A more-blocks-to-transfer value is calculated in a way that precludes transfer of any hot sectors in the buffer that are a part of a prefetch and are not yet actually requested by the host.

If the more-blocks-to-transfer value is greater than zero, then a request is made to increment the SCSI interface loop counter 123. A test is made as to whether such a change may be made in the counter 123, and if so, the loop counter 123 is incremented with the more-blocks-to-transfer value. This update of the counter 123 is carried out at this point in the program execution, so that the SCSI interface circuit 122 may continue sending blocks of data over the SCSI interface, even though the microcontroller 130 has shifted from the main loop phase to the servo phase. Then, the hot sectors register 262 of main memory is decremented by the number of sectors that have been incremented to the count held in the SCSI interface counter 123. A return is then made to the seek check logical node 232.

During execution of a read command process 226, it will be appreciated that the data sequencer process 234 will complete its task of locating data on the disk and transferring blocks into the cache 124 before the DMA

process 236 has completed sending that data on to the host via the SCSI interface circuit 122. During execution of the write command 224, just the opposite is true: the DMA process 236 will complete before the data sequencer process 234 is completed.

As illustrated in FIG. 1 1, the three main subprocesses, seek 232, data sequencing 234 and DMA transferring 236 are independent of each other and DMA transfers may be occurring simultaneously either with seek activity or with sequencer activity. While the data sequencing process 234 is independent of the DMA transfer process 236, the actions must be coordinated. Coordination occurs via the hot sectors register 262 and the sectors allocated register 268 of main memory. The hot sector register 262 informs the sequencing process 234 during write command execution that one or more sector blocks are available in the cache buffer 124 for transfer to disk. When these blocks are written to disk, the sequencing process uses the sectors allocated register 268 to inform the DMA transfer process 236 that holes have been created in the cache buffer 124 which are now available for additional blocks from the host, and the DMA process 236 then goes out to the host, obtains new blocks, causes them to be loaded into the cache buffer 124 and then increments the hot sectors register 262 to cause these blocks to be added to the count of sectors awaiting transfer to disk.

Thus, during the progress of a seek to a specified track location the cache buffer 124 is filling up with data blocks via the activity of the DMA process 236, and the hot sectors register 262 is incrementing. If the host transfer is larger than the cache buffer capacity, 16 sectors are loaded into the cache 124 and the DMA transfer process waits until one or more of these sectors is written to disk and a hole in the cache memory 124 becomes available before requesting any more data blocks from the host.

In the read command execution process 226 the hot sectors register 262 contains the count of the number of sectors that have been transferred from disk to buffer including prefetch sectors which lie in the track sequentially from the requested sectors but which have yet to be requested by the host. In the read process 226 the sectors allocated register 262 contains the count of the number of sectors that have been transferred via the DMA transfer process 236 to the host thereby creating holes in the cache buffer 124 for additional sectors to be read from disk.

Data is stored vertically in each cylinder location so that during a read operation it may be necessary to perform a head switch to the next head in order, which provides the next data track. When a head select is made, the seek active node 238 is true and the sequencer process 234 is inhibited during the head select process which is accomplished in a few microseconds. When it is necessary to move the actuator to the next cylinder, an angular microstep to the next adjacent track is typically commanded via the on track position servo and this condition also results in the seek active process 234 being true. A single track seek requires about six milliseconds to complete.

Here follows a listing in object code of a control program to enable the microcontroller 130 to carry out the control tasks described above. The first two digit positions following the leftmost colon in each line set forth the line character count "n". The next four digit positions set forth the memory address for the starting byte of the line, the next two digit positions are zero,

and the next "n" characters are the byte values of the program contained on the particular line. The last two

digit positions of each line comprise a check sum for the line.

## Microprocessor ROM 132



## External Program Memory 134

:20010000B90709F140E02C68803A8400B90709F140E02CE00070995EB812207D05082D390C  
 :20012000D824E8B970080399031F51B900513880FC3AFD0031CD09F0E2DB240109F0E3DB16  
 :2001400088C8585109F0E1DB5109F0E0DB5109F0DFDB5109F0DEDDB51B90A51B900515151D4  
 :20016000515C51B900515109F0F6DB5109F0F5DB5109F0F4DB515609F0F2DB240109F0F3AB  
 :20018000DB24C82D0D002F00D407FC086000D024C82D0D0009F1F3DBD009F1F2DB67BDDA9D  
 :2001A000BA0A1520208050207D50209A505628AF4D09F08DDA09F1E6DB09F08CDA09F1E78A  
 :2001C000DB09F0E5DB228A1C3009F1E9DBD009F1E8DB28814C6000002280228222411A260A  
 :2001E00022282287229229009F1F6DB09F1F4DB09F1F5DBBA0465DEDB1500BA0665E2DADF  
 :200200001500A19BA399A099A29AB79AA29BA39BA09BB1E9A2E9A49B09F0DED8C109F1E423  
 :20022000DBB90009F1A3DBB90209F1F8DBB9E009F106E0B9C009F10EE009F08DDA09F102F4  
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without departing from spirit and scope of the invention. The disclosure and the description herein are purely illustrative and are not intended to be in any sense limiting.

What is claimed is:

1. A disk drive subsystem including integral data block sequencer means, cache memory means and interface means for direct memory access interface with a host computing machine and further including a disk forming data storage surfaces, the disk being mounted to a spindle journaled to a base, an electromechanical head transducer actuator structure mounted to the base for moving a plurality of data transducer heads among a multiplicity of concentric data tracks formed on each data storage surface of the disk, the subsystem further comprising:

single, time divided multi-tasked digital supervisor means programmed for supervising track seeking, micro-stepping and following servo control operations of the actuator structure during a servo control phase of a two-phase operational cycle being a supervision phase devoted to supervision of data block handling functions of disk drive data block sequencer means, cache memory means and interface means, the digital supervisor means being programmed so that during track seeking and micro-stepping settle operational modes of the subsystem each said two-phase operational cycle of the supervisor means is of shorter time duration than the duration of a said two-phase operational cycle of the supervisor means during track following operational modes.

2. The disk drive subsystem as set forth in claim 1 wherein said digital supervisor is programmed so that during track seeking operations within a said two-phase operational cycle each servo control phase is approximately 60 microseconds in duration and each supervision phase is approximately 30 microseconds in duration, so that during track settling operations within a said two-phase operational cycle each servo control phase is approximately 80 microseconds in duration and each supervision phase is approximately 40 microseconds in duration, and so that during track following operations within a said two-phase operational cycle each servo control phase is approximately 75 microseconds in duration and each supervision phase is approximately 105 microseconds in duration.

3. The disk drive subsystem set forth in claim 1 wherein the supervisor means is programmed to perform the other supervision phase within a main loop.

4. The disk drive subsystem set forth in claim 1 wherein the single, time divided multi-tasked digital supervisor means comprises a microprocessor means including an internal readonly program memory means for storing first predetermined portions of a control program executed by the microprocessor means, and further comprising an external read-only program memory means for storing second predetermined portions of the control program executed by the microprocessor means.

5. The disk drive subsystem set forth in claim 4 wherein the first predetermined portions of the control program stored in the internal read-only program memory means include access-time-critical service routines, and wherein the second predetermined portions of the control program include non-timecritical service routines.

6. The disk drive subsystem set forth in claim 1

wherein the electromechanical head transducer actuator structure comprises a mass balanced, substantially in-line rotary actuator head positioner and further comprising a polyphase-providing position encoder coupled between the head positioner and the base for generating polyphase position information indicative of the position of the head positioner as it rotates relative to the base.

7. The disk drive subsystem set forth in claim 6 wherein the polyphase-providing position encoder comprises a optical transducer means having a moving scale attached to the head positioner and having light source means and a reticle-masked photodetector array means formed as a single module adjustably secured to the base, the optical transducer means for putting out plural phases relatively indicative of track position and direction of movement of the actuator structure.

8. The disk drive subsystem set forth in claim 7 wherein the moving scale and base and head positioner are comprised of materials having coefficients of thermal expansion which differ linearly over temperature change.

9. The disk drive subsystem set forth in claim 6 further comprising prerecorded data track centerline information in plural track locations on at least one said data storage surface.

10. The disk drive subsystem set forth in claim 9 wherein the digital supervisor means is programmed to calibrate the position encoder by reference to the prerecorded data track centerline information during a recurrent calibration service routine.

11. The disk drive subsystem set forth in claim 10 wherein the prerecorded data track centerline information is recorded in plural track locations at a radially outermost region and at plural track locations at a radially innermost region of each data surface, the centerline information being readable by the data transducer head positioned for reading data from that particular surface, and wherein the digital supervisor means includes analog to digital converter means and is connected to receive and process the position information from the position encoder during one phase of the two-phase operational cycle and wherein the digital supervisor means obtains and processes the centerline information from the disk surfaces read by the data transducer during the calibration service routine.

12. The disk drive subsystem set forth in claim 11 wherein each said track location corresponds to a said phase of the polyphase encoder thereby enabling separate calibration of each phase over the range of head positioner movement between the outer region and the inner region during a said calibration service routine.

13. The disk drive subsystem set forth in claim 12 wherein the digital supervisor means is programmed to calibrate during the calibration service routine the position information from the position encoder to centerlines of the data tracks by automatically commanding the actuator structure to seek to the outermost region and to store centerline information read form each track location for each encoder phase and for each data surface, to seek to the innermost region and to store centerline information read therefrom for each encoder phase and for each data surface, and to calculate and store from recorded inner and outer servo information for each encoder phase and for each surface a reference offset value and an angular slope value indicative of the difference in offset between the polyphase information and data track centerline servo information from the

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outermost region and the innermost region, and, during track following operations to follow the centerline of a data track located between the outermost and innermost regions by causing track following current to be supplied to the rotary actuator structure in response to the polyphase information as corrected by a particular track offset correction value derived from the stored reference offset value and the angular slope value.

14. The disk drive subsystem set forth in claim 13 wherein the data track centerline correction servo information comprises for a track within each region of each surface a single servo sector containing sequentially circumferential bursts including a first burst and a second burst, one of the bursts being offset radially in one direction of disk radius from the centerline of the track by a predetermined amount and the other of the bursts being offset radially in the other direction of disk radius from the centerline and further comprising peak detection circuitry connectable to the digital supervisor means so that the relative magnitudes of each of the bursts may be converted to digital values and stored for further processing by the supervisor means.

15. The disk drive subsystem set forth in claim 14 wherein each servo sector of a track location on a surface is circumferentially displaced from every other servo sector of the other surfaces at the same track location so that all sectors for all surfaces may be read and processed by the supervisor means during a single rotation of the disks.

16. The disk drive subsystem set forth in claim 14 wherein the digital supervisor means is programmed to determine during the calibration service routine and to store a read channel automatic gain compensation value by averaging burst servo amplitudes of all heads as read from the outermost region while following track centerline and averaging burst servo amplitudes of all heads as read from the innermost region and by storing an ACG reference and slope value to compute therefrom an AGC value for a particular cylinder location.

17. The disk drive subsystem set forth in claim 10 wherein the digital supervisor means is programmed to determine and record seek direction hysteresis error values for the head positioner during long seeks during the recurrent calibration service routine.

18. The disk drive subsystem set forth in claim 10 further comprising a temperature sensor for sensing temperature of the base at the vicinity of the position encoder.

19. The disk drive subsystem set forth in claim 18 wherein the supervisor means is programmed to scan periodically the temperature sensor and to store sensed temperature, and automatically to repeat the calibration service routine upon detection of a change of predetermined magnitude of sensed temperature of the base above a threshold value.

20. The disk drive subsystem set forth in claim 1 wherein the digital supervisor means is programmed to determine and store a head gain coefficient which is

related to the width of each data transducer head by commanding the actuator structure to shift a predetermined distance from track centerline of each track containing a predetermined pattern of radially offset servo bursts therein and thereupon to read and record the amplitude of each said burst and thereupon calculate an average value of burst amplitude centerline information read from an outermost track region while following track centerline and while offset therefrom and then to repeat this foregoing determination at the innermost track region in order to obtain and record a slope value for each head and thereupon calculate a head gain value for each head to determine for each head the positional compensation required in order to move the particular head into precise centerline alignment with each track to be followed thereby.

21. The disk drive subsystem including integral data block sequencer state machine means, cache memory means and interface state machine means for direct memory access interface with a host computing machine and further including a at least one data storage disk forming data storage surfaces, the disk being mounted to a spindle journaled to a base, an electromechanical head transducer actuator structure mounted to the base for moving a plurality of data transducer heads among a multiplicity of concentric data tracks formed on each data storage surface of disk, the subsystem further comprising:

single, time divided multi-tasked digital supervisor means programmed for supervising track seeking, micro-stepping and track following servo control operations of the actuator structure during a first, servo control phase of a twophase operational cycle, another phase of each said two-phase operational cycle being devoted to supervision of data block handling functions of disk drive data block sequencer state machine means and interface state machine means,

the data block sequencer state machine means having sequencer loop counter means and the interface state machine means having interface loop counter means directly accessible by the digital supervisor means during the other phase of said two-phase operational cycle so that counts contained in said counter means may be updated during said another phase, thereby enabling each of said data block sequencer state machine means and interface state machine means to continue to loop through the states thereof while said digital supervisor means performs servo control operations during said first, servo control phase.

22. The disk drive subsystem set forth in claim 21 wherein said data block sequencer state machine means and said interface state machine means communicate block transfer status of, and storage availability within, said cache memory means via hot sector and sector to go registers within said digital supervisor means.

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